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REMOTE-TERMINAL EMULATOR (DESIGN VERIFICATION MODEL)— DESCRIPTION OF HARDWARE

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The Remote-Terminal Emulator is a minicomputer-based system which generates message traffic for use in testing and evaluating large-scale multi-terminal computer systems. This series of reports describes the two Design Verification Models that were developed on Data General NOVA 800 minicomputers. This volume describes the hardware for the fixed-site and on-site emulators, with emphasis on the special purpose components developed for the emulator application. Design and implementation details are presented to facilitate maintenance and repair of both systems, and to facilitate field

20. Abstract (Cont)

modifications to the on-site system.

PREFACE

The Remote-Terminal Emulator is a minicomputer-based system which generates message traffic for use in testing and evaluating large-scale, on-line computer systems. In real-time testing, it emulates the actions of a collection of operators, terminals, and, depending upon configuration, modems. In 1972 and early 1973, two Design Verification Models (DVM) of the emulator were developed by The MITRE Corporation under the sponsorship of the Air Force Directorate of Automatic Data Processing Equipment Selection (MCS), the Electronic Systems Division of the Air Force Systems Command, and the Deputy for Command and Management Systems. The fixed-site system, which is used primarily for program and scenario development, is located at MITRE/Bedford and interfaces with the computer system under test (SUT) through the switched telephone network. The on-site system, which is used primarily for detailed emulator test and evaluation, is representative of the equipment planned for operational use in future computer procurements. This system, which is moved to each SUT site, interfaces through cables directly with the SUT's communication line adapters.

The primary hardware components of each of these systems are a Data General NOVA 800 minicomputer, a fixed-head disk, a magnetic tape unit, a control teletype, and an appropriate emulator/SUT interface unit. Both DVM's have sufficient hardware to emulate up to 16 low-speed interactive terminals. The on-site DVM also has hardware to emulate eight additional terminals or terminal networks by the use of high-speed synchronous line adapters and associated circuitry. The primary software components that have been developed for this project consist of the Marco Preprocessor, the Scenario Assembler, the Real-Time Executive, the Scenario Interpreter and the Data Reduction Program.

The common denominator of remote-terminal emulation is the scenario, which is a program that controls the actions to be taken by the emulator in emulating a given device and mix of devices. The

scenario defines the queries (system commands, input data, and control characters) to be sent to the SUT, how SUT responses are to be processed, and other details of the test to be conducted. The Macro Preprocessor is a general purpose support program that provides a basic macro capability to aid in scenario writing and which was also used in emulator program development. In the scenario development process, the Scenario Assembler is used to convert external (symbolic) scenarios to internal (absolute) scenarios which are tailored to a specific terminal type and to specific data communications control procedures. Both the Macro Preprocessor and the Scenario Assembler run under the Data General Disk Operating System (DOS). In real-time testing, internal scenarios are brought into core from disk and are processed by the Scenario Interpreter which runs under the Real-Time Executive. All messages sent to and received from the SUT, as well as messages describing other actions of the emulator, can be time-tagged and logged on magnetic tape. Upon completion of the test, these data are processed in various fashions by the Data Reduction program (which also runs under DOS) to produce scenario trace data and various statistics on the performance and utilization of both the emulator and the SUT.

This document is part of a series of reports which describe the design, implementation and use of the two Design Verification Models. The titles of the reports in the series are as follows:

Volume	Title
1	Introduction and Summary
2	Scenarios and Data Structures
3	Macro Preprocessor
4	Scenario Assembler
5	Scenario Interpreter
6	Real-Time Executive
7	Data Reduction Program
8	Hardware

9	Support Software
10	User's Manual

It is suggested that the reader become familiar with the emulator concepts and terminology presented in Volume 1 preparatory to reading other volumes in the series.

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INTRODUCTION

The Remote-Terminal Emulator is a minicomputer-based system which generates message traffic for use in testing and evaluating large-scale, on-line computer systems. In real-time testing, it emulates the actions of a collection of operators, terminals, and, depending upon configuration, modems. In 1972 and early 1973, two Design Verification Models (DVM) of the emulator were developed by The MITRE Corporation under the sponsorship of the Air Force Directorate of Automatic Data Processing Equipment Selection (MCS), the Electronic Systems Division of the Air Force Systems Command, and the Deputy for Command and Management Systems. The fixed-site emulator, which is used primarily for program and scenario development, is located at MITRE/Bedford and interfaces with the computer system under test (SUT) through the switched telephone network. The on-site emulator, which is moved to each SUT site, interfaces through cables directly with the SUT's communication line adapters.

The equipment used in these two emulators is described in this volume, with emphasis on the on-site emulator since this is representative of the system planned for future use by MCS. As will be seen, the principal difference between the on-site and the fixed-site emulators is in the communications equipment used to connect the emulator to the SUT.

Section II describes the equipment used in the on-site emulator, with emphasis on the special purpose components developed for the emulator application. Section III describes the system configuration and the communications subsystem of the fixed-site emulator. Design and implementation details are documented to facilitate maintenance and repair of both systems and to facilitate emulator/SUT interfacing.

SECTION II

ON-SITE EMULATOR

SYSTEM CONFIGURATION

The system configuration for the on-site emulator is shown in Figure 1. The Central Processing Unit (CPU) is a Data General NOVA 800 with direct memory access in addition to normal programmed I/O. During emulator development, the system contained 24K words (16-bits per word) of core memory and 256K words of secondary storage (fixed-head disk); in later test phases, the memory was expanded to 28K as shown in the figure. The disk is used for storing systems and applications programs as well as scenarios that are transferred into core for a real-time emulation run.

The teletype is used for system control during an emulation run. It can also be used for editing data or program files. The paper tape reader is used to enter hardware diagnostics. The magnetic tape unit is used for off-line file storage of programs and scenarios; it is also used to log emulator and SUT data during a real-time run. The printer is used for core dumps, program and scenario listings, and to print test data from the log tape. The Readable Real-Time Clock (RRTC), Interval Timer (IT) and Real Time Clock are used for task scheduling and timing.

Line adapters allow for interfacing up to 64 asynchronous and 8 synchronous transmit and receive lines. The digital I/O boards support the line adapter interfaces by supplying all control signals necessary to mimic the actions of modems. All the asynchronous line adapters operate independently with respect to baud rate, character length, and number of start/stop bits.

All components of this system were purchased from Data General Corporation with the following exceptions: Readable Real-Time Clock

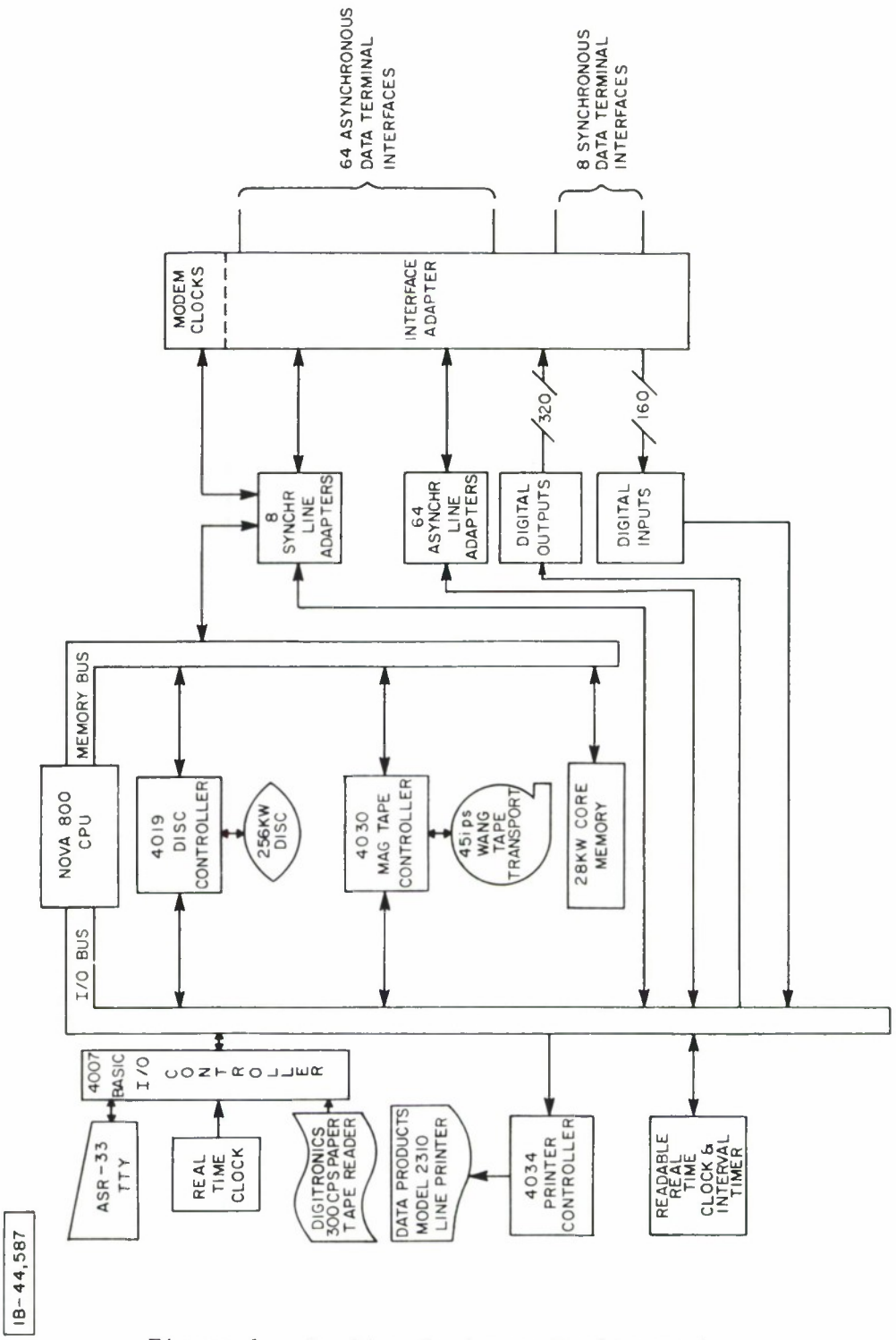


Figure 1. On-Site Emulator Configuration

and Interval Timer, and Interface Adapter, which were designed and implemented by MITRE, and the asynchronous and synchronous line adapters, which were purchased from Digital Computer Controls Corporation.

The following discussion briefly describes the less standard components of the system. More detailed descriptions of these components as well as the remainder of the system hardware can be found in the manuals listed in the bibliography at the end of this report.

COMMUNICATIONS EQUIPMENT

To provide the emulator with program control over interface signals, the EIA control signals are generated by digital input/output boards. EIA data signals are processed by Asynchronous and Synchronous Line Units (ALU's and SLU's) produced by Digital Computer Controls Corporation. All EIA control signals are tied true on these boards so they will not interfere with the emulator operation.

Timing signals for the Synchronous Line Units are provided by modem clocks developed by The MITRE Corporation and contained in the Interface Adapter. Detailed descriptions of these special-purpose devices are contained in Appendix B.

Digital Input Boards

The digital input boards used in the on-site NOVA were designed by Data General's special products group. Each board converts 32 EIA signals to 32 TTL signals to be read onto the NOVA's I/O bus, and into core memory. A DIA instruction will select the high-order 16 lines and transfer them to the selected accumulator. A DIB instruction will transfer the low-order 16 lines to the selected accumulator. Figure 2 is a simplified diagram of digital input circuits.

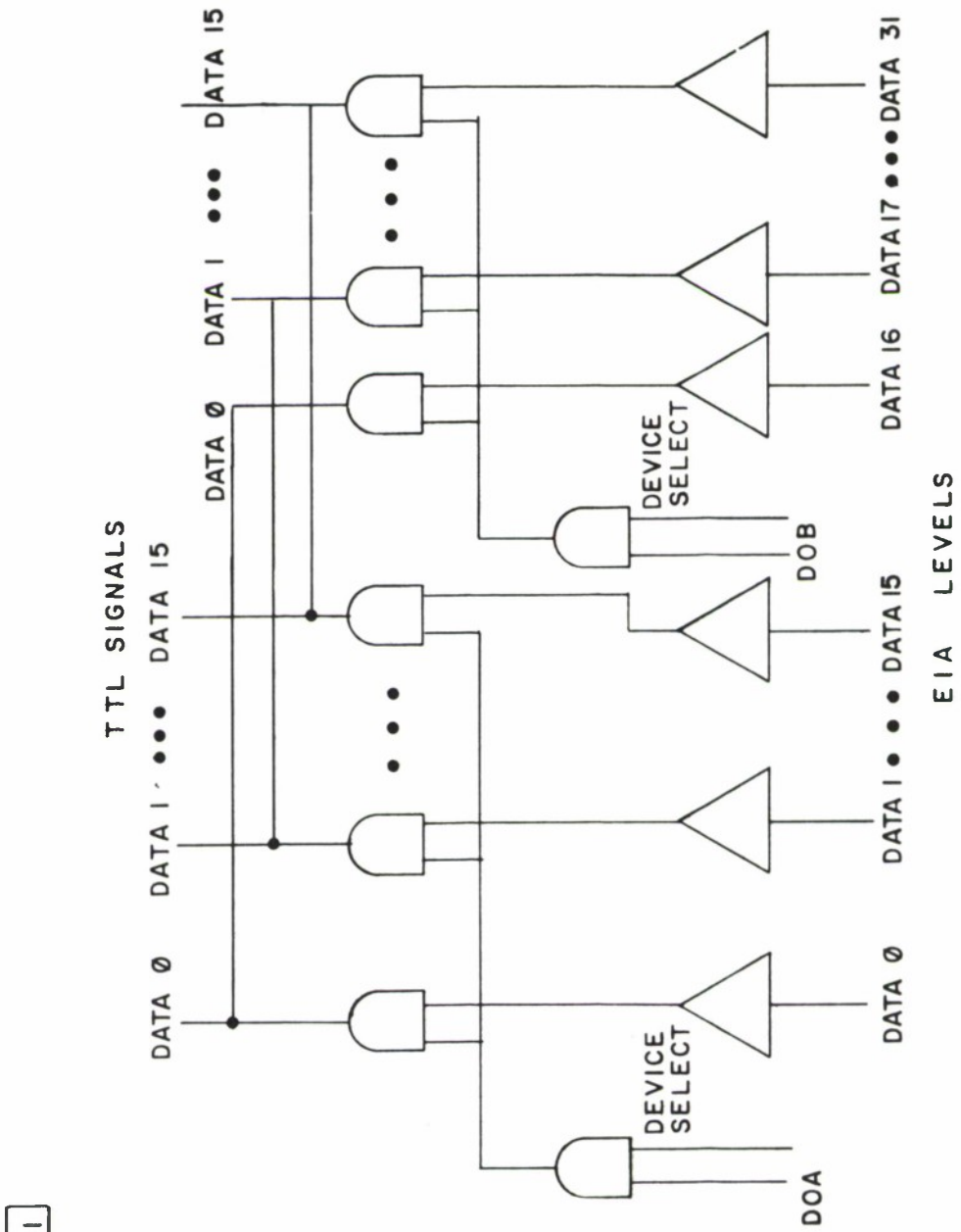


Figure 2. Simplified Diagram of Digital Input Circuits

Digital Output Boards

The digital output boards were also designed by Data General's special products group. They convert the TTL signals from the NOVA's I/O bus to EIA signals. A DOA instruction loads the high-order half of a 32-bit register with the contents of the selected accumulator, while a DOB instruction loads the low-order half of the register. The outputs of these registers are converted to EIA standard signals used to mimic modem control output signals. Figure 3 is a simplified diagram of digital output circuits.

Asynchronous and Synchronous Line Adapters

Line adapters were manufactured by Digital Computer Controls Corporation (DCC). Both are character-oriented (as opposed to bit oriented), I/O data communications controllers. All EIA control lines have been jumpered true; therefore, the line adapters are used only for data. Asynchronous line adapters are packed eight to a board, while synchronous line adapters are packed four to a board.

Asynchronous Line Adapters

Several options can be selected via straps on the asynchronous line adapter board - 1, 1½, 2, or 2½ stop bits; odd, even, or no parity; from 6 to 8 data bits; and up to 19.2K baud rates. All options are separately selectable for each channel of each line adapter.

Baud rates are generated from one of two clock circuits on the line adapter boards. One of these provides the 110 baud clocking; the other handles multiples of 150 baud, up to 19.2K baud. Baud rates are selected for each of the units on a board, and provisions are made for transmitting and receiving at different baud rates.

Non-standard (to DCC) baud rates can be installed by changing the crystal in either clock circuit by the formula FREQ = 40960 x the desired baud rate.

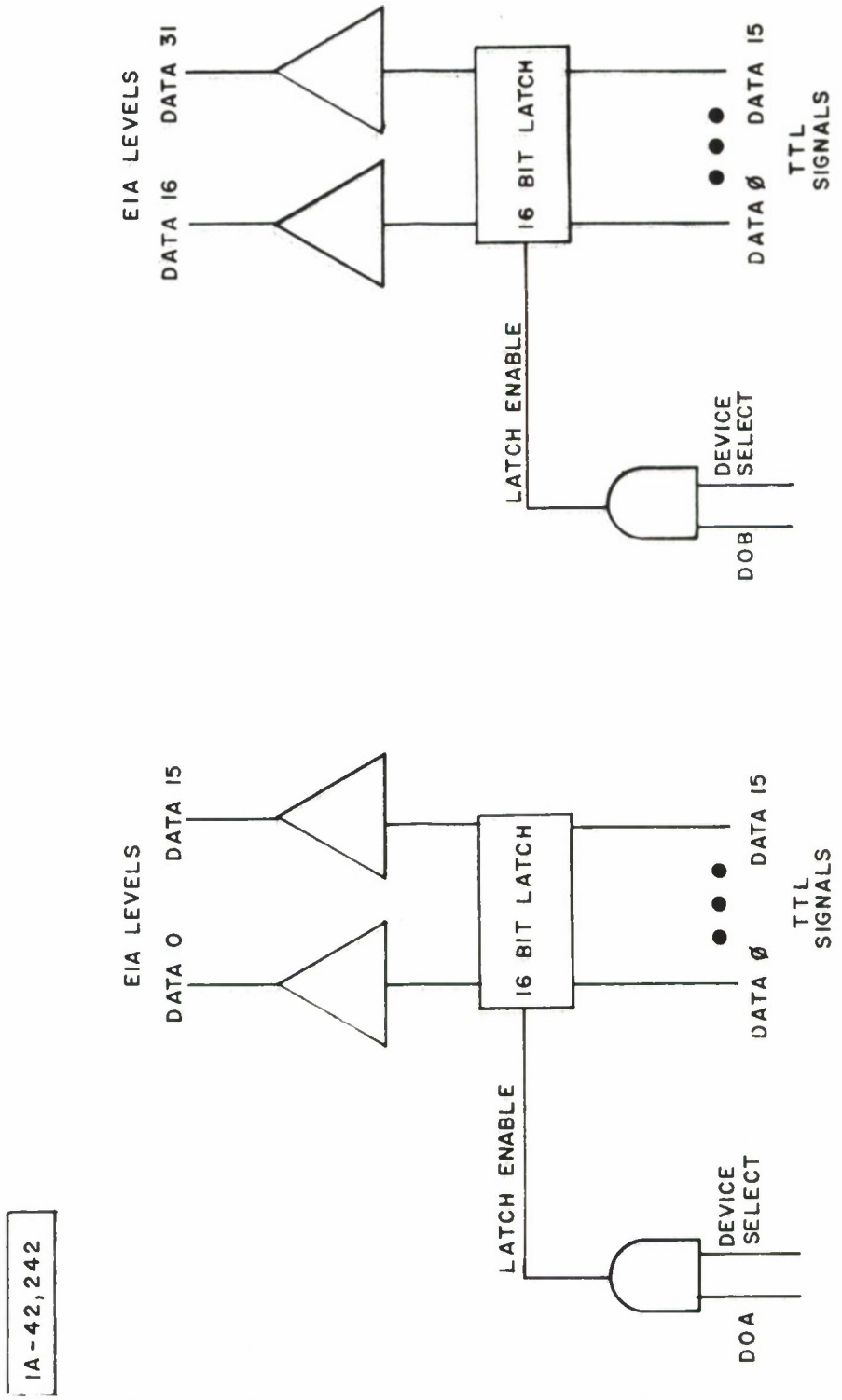


Figure 3. Simplified Diagram of Digital Output Circuits

A switch was installed on two of the ALU boards to select one of these "non-standard" frequencies. The switch selects a crystal that provides 134.5 baud clocking (instead of the 110 baud) which is the correct frequency for IBM 2741 emulation.

Data transfers to and from the ALU's are performed with programmed I/O.

Synchronous Line Adapters

Synchronous line adapters are packed 4 to a board and afford strap options independently for the transmit and receive sections. The strap options include a 5 - 8 bit character, and even, odd, or no parity. Internal clocking provides clocking from 2.4KB to 153.6KB. External clocking is available from the modem clocks discussed later in this section.

Data transfers to and from the SLU's use the direct memory access channel.

INTERFACE ADAPTER

Description

The purpose of the interface adapter (rack) is to provide enough flexibility for a wide variety of SUT interface requirements. To achieve this, the internal wiring of the interface adapter is done with temporary jumpers.

All the signals to and from the NOVA are cabled onto barrier strips in the interface adapter. The front of the interface adapter contains an array of 72 25-pin connectors, used to connect to the SUT. These connectors are wired to a second set of (24-pin) barrier strips within the interface adapter. Pin 2 on the barrier strip connects to pin 2 on the connector, pin 3 on the barrier strip connects to pin 3 on the connector, etc.

Four of the five modules in the interface adapter have sixteen sets of these barrier strips and sixteen connectors. In addition to this, each module has a barrier strip containing power and clock pulses (the latter for use with the synchronous adapters). The fifth module contains 8 sets of barrier strips plus the clock barrier strip. This same module contains power and clock circuitry.

Two light-emitting diode displays are associated with each SUT connector and are usually used to monitor data transmissions. They are wired via jumpers and will light up for 1/10th of a second whenever a true signal (+12VDC) is applied to them.

Interconnections

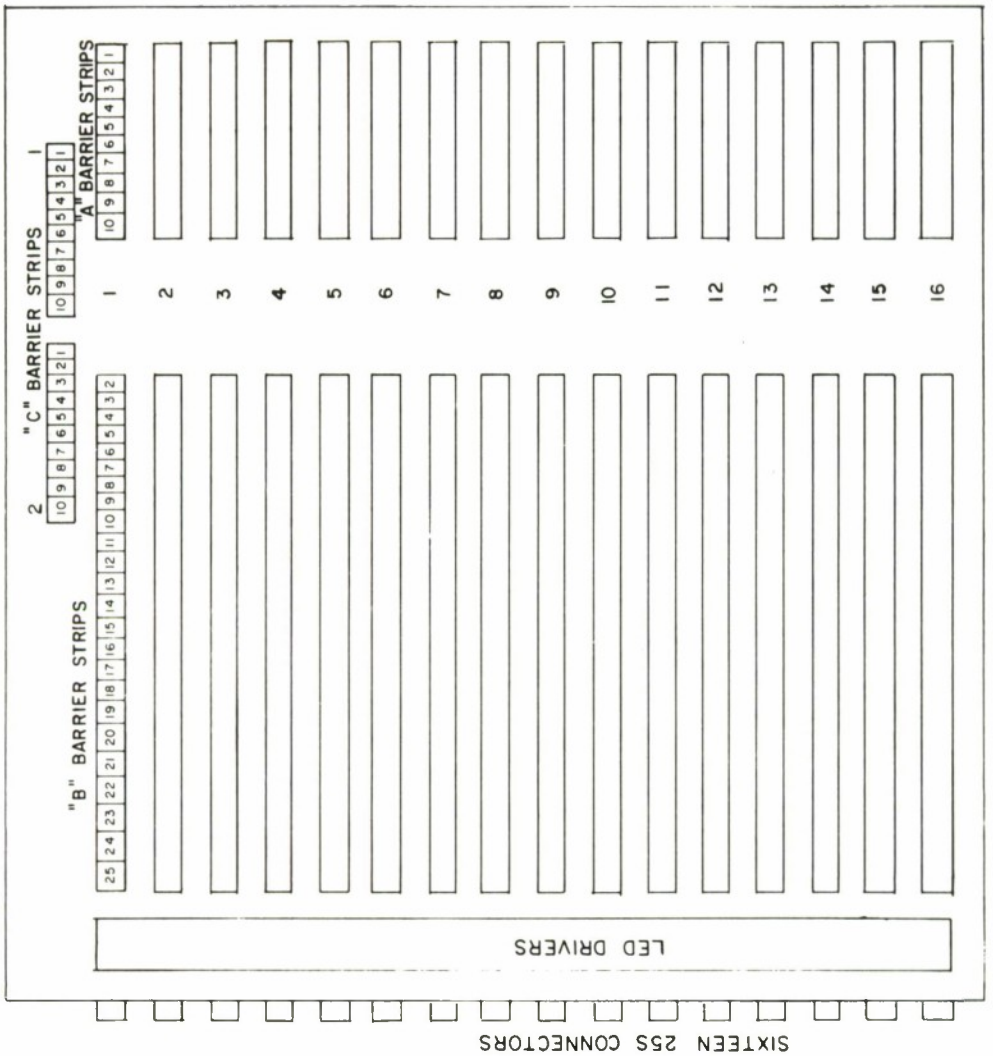
Figure 4 shows the mechanical layout of an interface adapter module. Barrier Strips "A" are cabled to the NOVA; Barrier Strips "B" are wired to the SUT connectors; and Barrier Strips "C" provide clocking and power connections. The typical jumper connections between the A and B Barrier Strips for low-speed asynchronous modems are shown in Figure 5.

Appendix A contains the wiring lists of all wiring between the NOVA and the SUT connectors. Also included in Appendix A is Table I, which shows the correlation between interface connectors and device codes, where they have been assigned.

MODEM CLOCKS

Oscillators mounted in the interface adapter provide frequencies from 150 baud to 9600 baud for use with synchronous communications. The frequencies that are available on "C" barrier strips are pictured in Figure 5.

A detailed circuit description, with a table of the available frequencies, may be found in Appendix B.



18-42,243

Figure 4. Interface Adapter Module

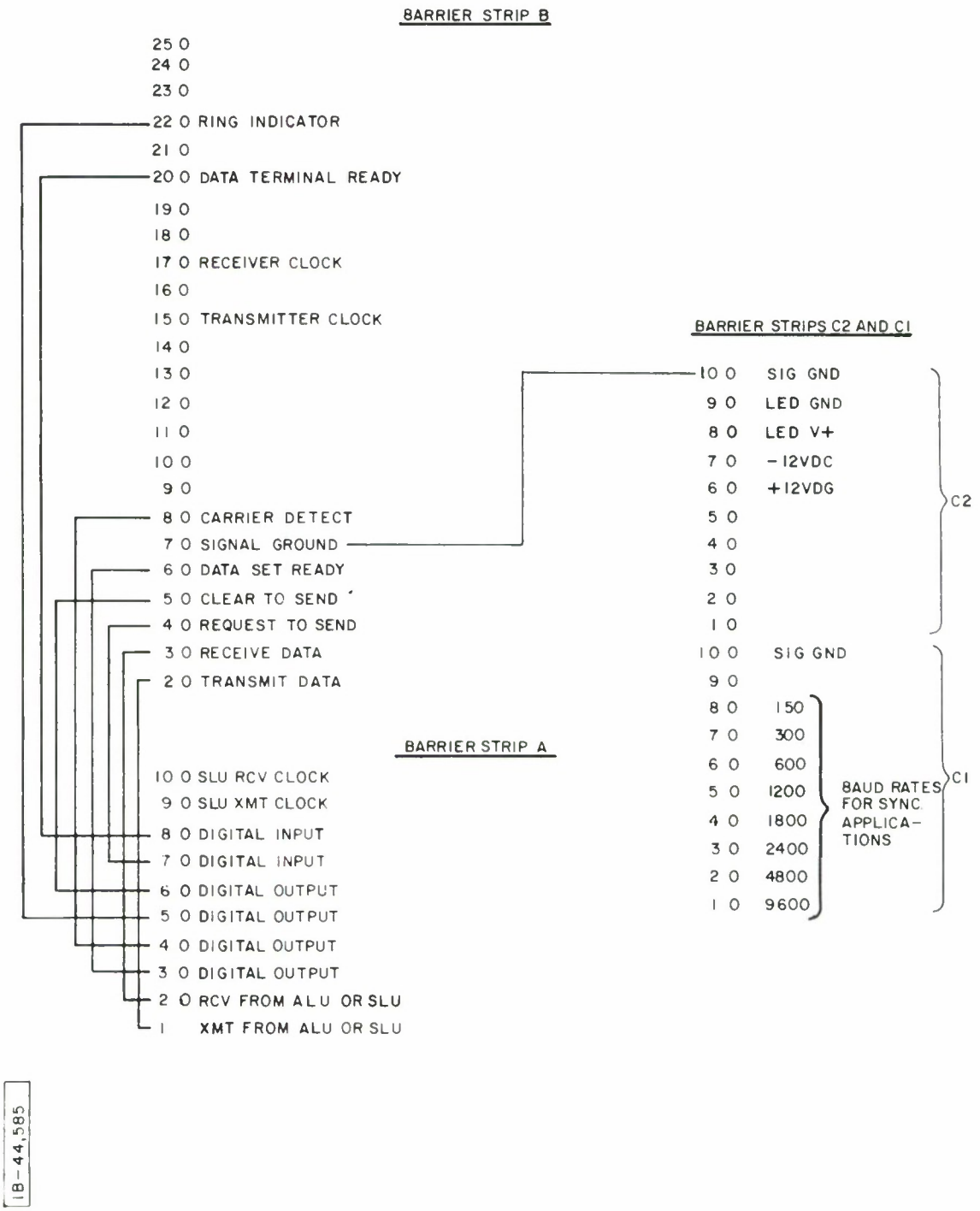


Figure 5. Barrier Strip Lug Assignments and a Typical Jumper Configuration

INTERVAL TIMER AND READABLE REAL-TIME CLOCK

General Description

The IT and RRTC allow a user to make precise measurements of time intervals or to establish precise time intervals.

The interval timer is a 16-bit latch that is loaded by a DOA instruction and read by a DIC instruction. When loaded with a value, the IT will count down to zero (until it carries) which will generate an interrupt if interrupts are enabled. The IT is stepped at 1 ms intervals and will hold a maximum count equal to 65.5 seconds.

The RRTC is a 32-bit latch connected to a 32-bit binary counter. The counter can be reset by issuing a DOC instruction. Data is transferred from the counter to the latch via an I/O pulse. DIB will put the latch's low-order 16 bits on the I/O bus, and DIA will present the high-order 16 bits to the I/O bus. (If no I/O pulse was sent to the RRTC between the DIA and DIB, the two 16-bit words represent the count at the time of the last I/O pulse.) The clock is stepped every 10 us and will hold a maximum count approximately equal to 12 hours.

A complete description of the circuit and diagnostic programs is given in Appendix C.

SECTION III

FIXED-SITE EMULATOR

SYSTEM CONFIGURATION

The system configuration for the fixed-site emulator is shown in Figure 6. As with the on-site emulator, the CPU is a Data General NOVA 800. During the emulator development phase, the fixed-site emulator had 28KW of core ememory. The teletype, paper tape reader, line printer, disk and timing units for the fixed-site emulator are identical to those used in the on-site system.

The fixed-site emulator which was used in the development of the applications software and test scenarios differed from the on-site emulator principally in the communications equipment since the fixed-site emulator interfaces with various SUT's over the switched telephone network, whereas the on-site emulator connects directly to the SUT's line adapters. The synchronous line adapter and modem were incorporated into this system for use in preliminary tests of polling scenarios and scenarios for emulation of remote-batch terminals. The asynchronous line adapters and modems were used for preliminary tests of scenarios for emulation of low-speed interactive terminals such as the IBM 2741 and teletypes.

The card reader shown in Figure 6 is for source data entry of application programs and scenarios. A card reader was not included in the on-site emulator for cost and size reasons. Application program maintenance and scenario development are normally accomplished using the fixed-site emulator. Updated programs and scenarios are then transferred to the on-site emulator by way of magnetic tape.

All components shown in Figure 6 were purchased from Data General Corporation with the following exceptions: the 16 low speed modems (7103's) were purchased from the Teledynamics Corporation;

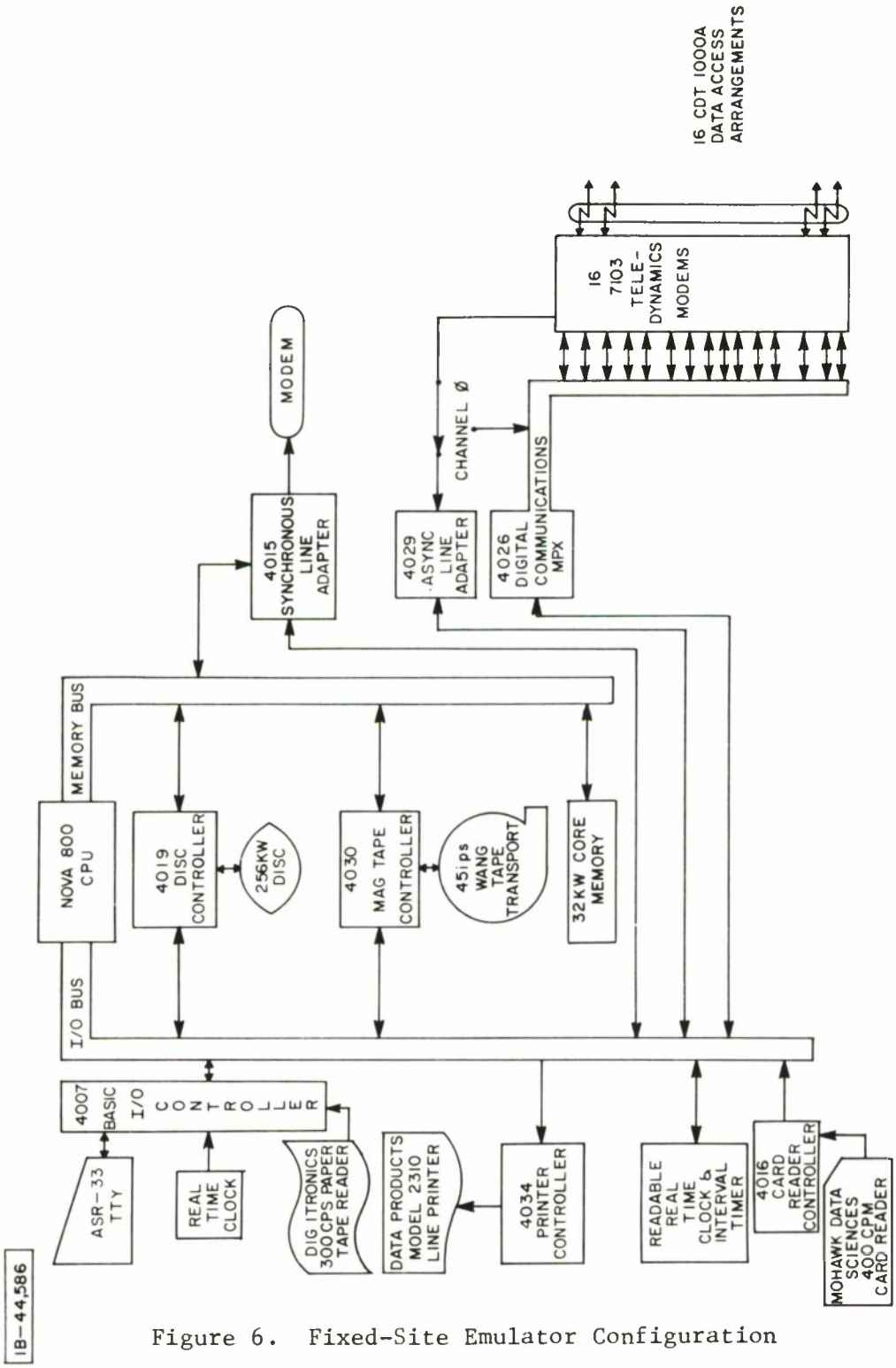


Figure 6. Fixed-Site Emulator Configuration

the 201 modem, and 16 DAA's were leased from the Bell Telephone Company; the Readable Real-Time Clock and Interval Timer were provided by The MITRE Corporation.

COMMUNICATIONS EQUIPMENT

Line Adapters

Communications equipment includes a 4015 high-speed Synchronous Line Adapter (50K baud), a switchable speed (110-2400 baud) 4029 Asynchronous Line Adapter (ALA), and a 16-line 4026 Digital Communications Multiplexor (DCM). The DCM will operate at 110 baud or 134.5 baud. All sixteen channels of the DCM share the same clock and must, therefore, operate at the same frequency.

The ALA and DCM share sixteen Teledynamics model 7103 modems (a Bell System 103 equivalent), which are connected to Bell System CDT1000 Data Access Arrangements (DAA's). These allow up to sixteen simultaneous, full-duplex transmissions using 16 of the 17 channels of the DCM and the ALA on the Centrex, local telephone, or Direct Distance Dial (DDD) networks. The ALA is limited to a maximum speed of 300 baud by the modems. The Synchronous Line Adapter interfaces to the phone lines via a Bell System model 201A modem.

NOVA Communication Interfaces

To allow flexibility in connecting external devices, all connections between the NOVA's asynchronous line adapters and modems are made via barrier strips. Each modem is hard wired to a DAA. Figure 7 shows a typical NOVA-to-phone line connection.

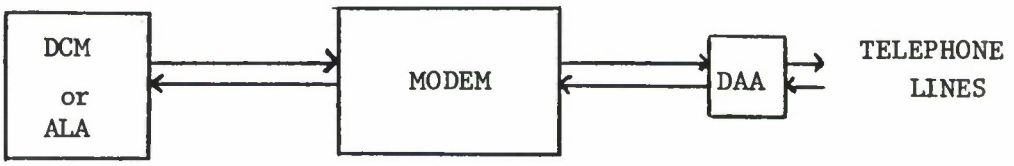


Figure 7. NOVA-to-Phone Line Connections

In addition to this wiring, a switch was installed, as illustrated in Figure 8, to allow DCM lines 14 and 15 (the last two lines of the DCM board) to be disconnected from their modems and cross coupled (i.e., XMT_{14} to RCV_{15} and XMT_{15} to RCV_{14}).

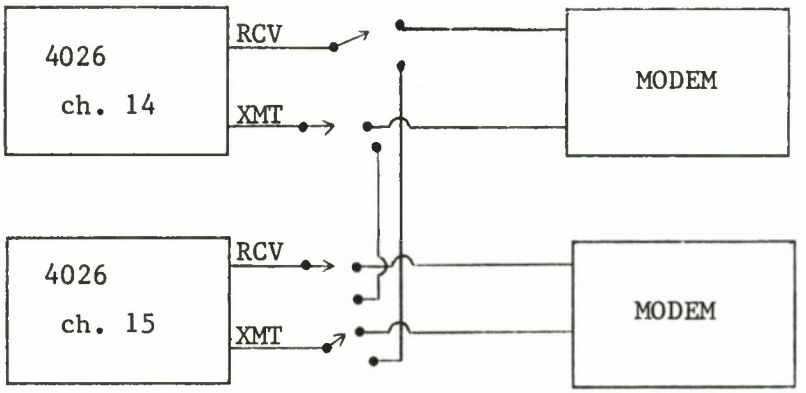


Figure 8. Cross Coupling Switch on DCM Channels 14 and 15

Teledynamics Modems

The Teledynamics model 7103 modems have test switches built in so that one of three modes of operation can be achieved. The switch positions for this modem are illustrated in Figure 9.

The "local" position connects the modem signals DT and DR; the "normal" position leaves the modem in normal operation; and the "digital loop back" position connects the digital signals BA and BB.

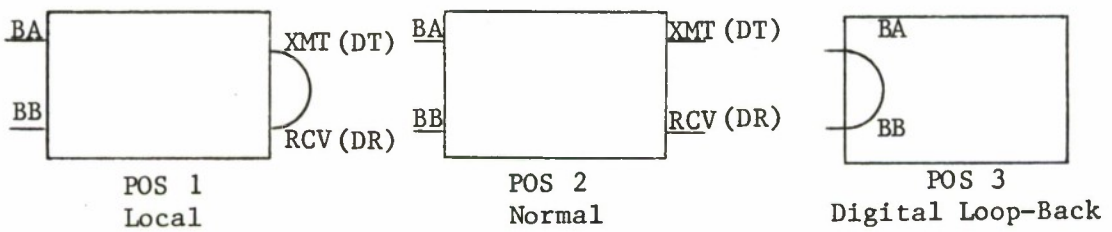


Figure 9. Switch Positions for Teledynamics Modems

APPENDIX A

WIRING LISTS FOR THE ON-SITE EMULATOR

The interface adapter is divided into five modules. Each of these is wired similarly except the top module, which has 8 sets of barrier strips and connectors, instead of 16.

Figure 10 shows the topography of an interface adapter module. Figure 11 shows emulator signal origins. Each of the barrier strips is situated with its lowest numbered pin toward the rear of the module. Barrier strips are numbered 1 through 16, from right to left as viewed from the rear.

The front panel consists of sixteen 25-pin connectors and 32 LED's. The circuitry for driving the LED's is mounted just behind the front panel and is not shown. The signal leads for each LED extend to the rear of the module and terminate in a spade lug that will mate with the lugs on the barrier strips.

The rear panel houses six connectors (S1 - S6). These are used to connect the cables which carry signals to and from the NOVA.

Soldered wiring is installed between barrier strips B and the front panel connectors, such that barrier strip B_K pin N is connected to connector P_K pin N. Wires are also soldered between barrier strips A and the connectors on the back panel. Complete lists for all wiring may be found at the end of this appendix.

Each cable used to connect the NOVA to the interface adapter is a 50-lead, single-wire shielded cable. In most cases, 32 wires are used and 18 are spares. Two connectors contain digital output signals (64 required for each module); one contains digital input signals (32 required for each module), and one carries data signals from the ALU or SLU, depending on which type of communications is being used in the module and one cable carries timing signals if synchronous

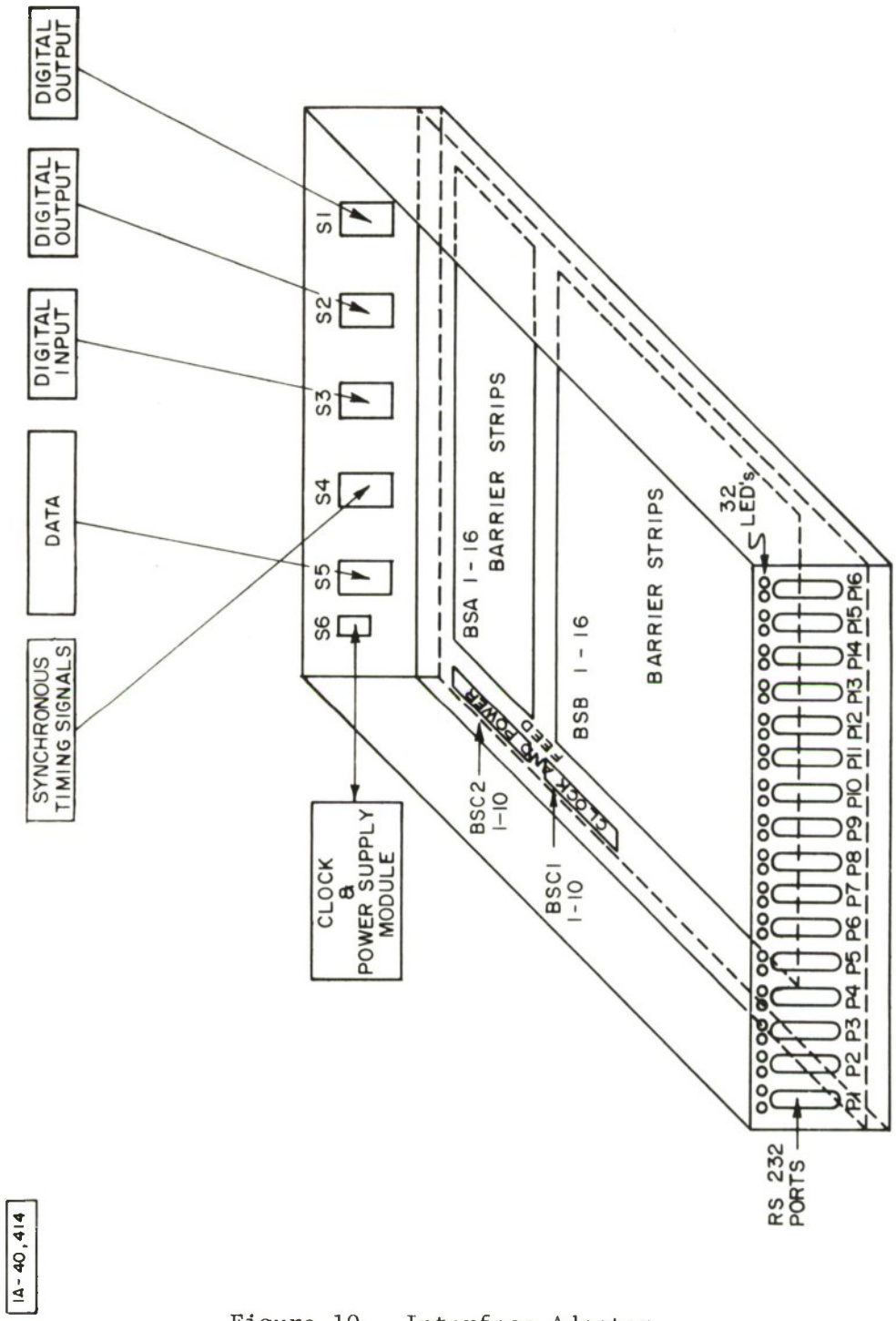


Figure 10. Interface Adapter

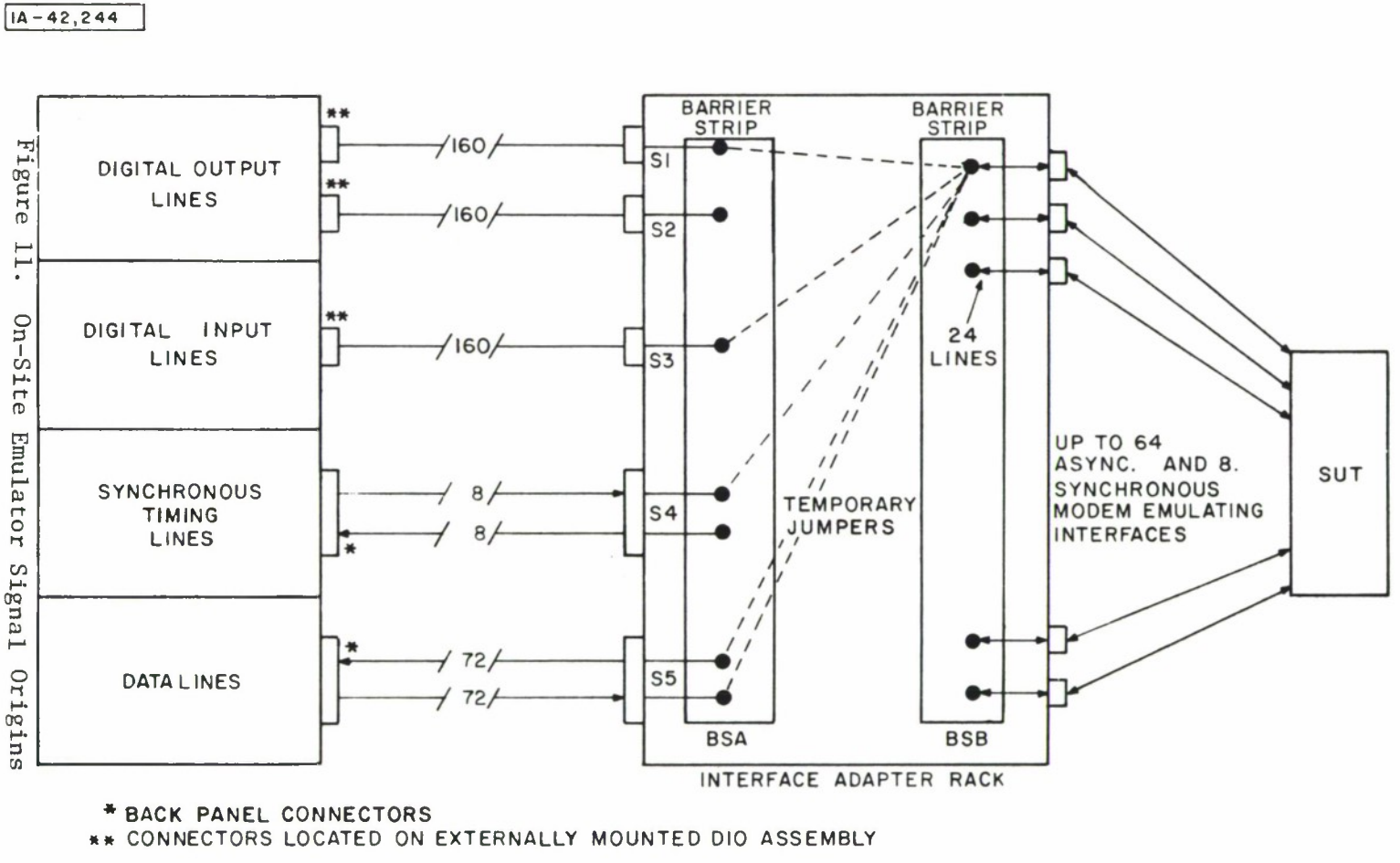


Figure 11. On-Site Emulator Signal Origins

communication is used. Clock and power signals are routed through S6 from the top interface module to BSC. Connector assignments are as follows:

S1 digital output lines

S2 digital output lines

S3 digital input lines

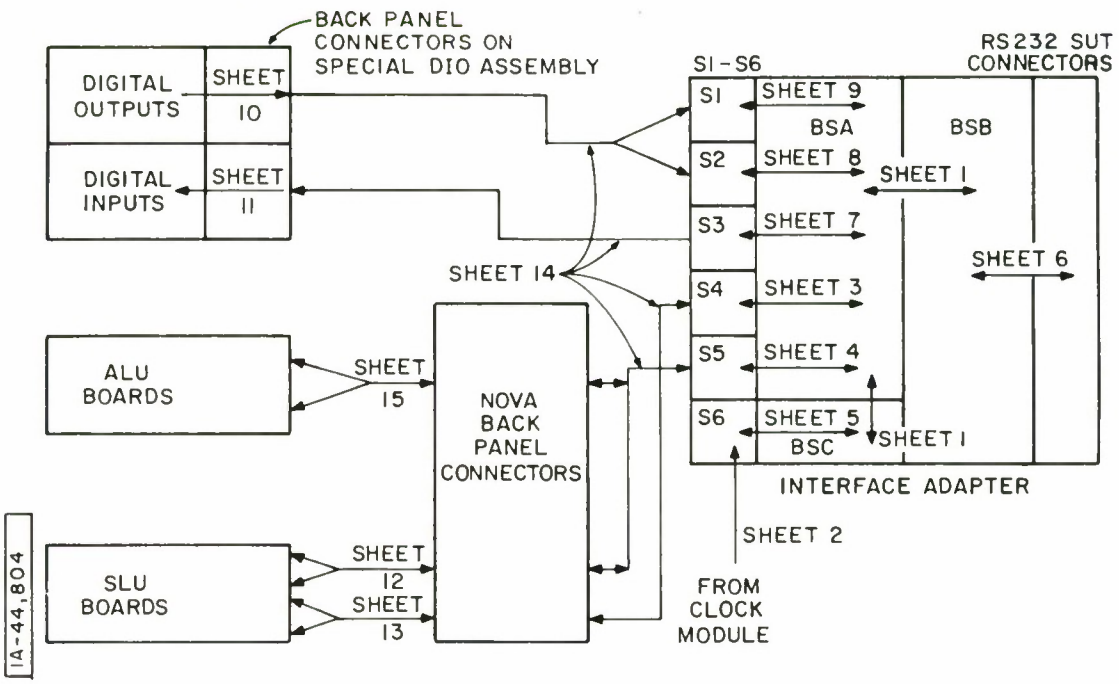
S4 synchronous timing signals

S5 data signals

S6 clock and power supply signals

Signal assignments on the barrier strips were described in Section II.

Table I describes the device codes assigned to the front panel connectors.



WIRING DIAGRAM DIRECTORY

Table I

Device Code Assignments

Connector	ALU/SLU RCV	ALU/SLU XMT	Digital* Input	Digital* Output
1			72 0,1 A	60 0-3 A
2			72 2,3 A	60 4-7 A
3			72 4,5 A	60 8-11 A
4			72 6,7 A	60 12-15 A
5			72 8,9 A	60 0-3 B
6			72 10,11 A	60 4-7 B
7			72 12,13 A	60 8-11 B
8			72 14,15 A	60 12-15 B
17	40	41	73 0,1 A	62 0-3 A
18	40	41	73 2,3 A	62 4-7 A
19	40	41	73 4,5 A	62 8-11 A
20	40	41	73 6,7 A	62 12-15 A
21	40	41	73 8,9 A	62 0-3 B
22	40	41	73 10,11 A	62 4-7 B
23	40	41	73 12,13 A	62 8-11 B
24	40	41	73 14,15 A	62 12-15 B
25	42	43	73 0,1 B	63 0-3 A
26	42	43	73 2,3 B	63 4-7 A
27	42	43	73 4,5 B	63 8-11 A
28	42	43	73 6,7 B	63 12-15 A
29	42	43	73 8,9 B	63 0-3 B
30	42	43	73 10,11 B	63 4-7 B
31	42	43	73 12,13 B	63 8-11 B
32	42	43	73 14,15 B	63 12-15 B
33	44	45	74 0,1 A	64 0-3 A
34	44	45	74 2,3 A	64 4-7 A

Table I (Continued)

Device Code Assignments

Connector	ALU/SLU RCV	ALU/SLU XMT	Digital* Input	Digital* Output
35	44	45	74 4,5 A	64 8-11 A
36	44	45	74 6,7 A	64 12-15 A
37	44	45	74 8,9 A	64 0-3 B
38	44	45	74 10,11 A	64 4-7 B
39	44	45	74 12,13 A	64 8-11 B
40	44	45	74 14,15 A	64 12-15 B
41	46	47	74 0,1 B	65 0-3 A
42	46	47	74 2,3 B	65 4-7 A
43	46	47	74 4,5 B	65 8-11 A
44	46	47	74 6,7 B	65 12-15 A
45	46	47	74 8,9 B	65 0-3 B
46	46	47	74 10,11 B	65 4-7 B
47	46	47	74 12,13 B	65 8-11 B
48	46	47	74 14,15 B	65 12-15 B
49	50	51	75 0,1 A	66 0-3 A
50	50	51	75 2,3 A	66 4-7 A
51	50	51	75 4,5 A	66 8-11 A
52	50	51	75 6,7 A	66 12-15 A
53	50	51	75 8,9 A	66 0-3 B
54	50	51	75 10,11 A	66 4-7 B
55	50	51	75 12,13 A	66 8-11 B
56	50	51	75 14,15 A	66 12-15 B
57	52	53	75 0,1 B	67 0-3 A
58	52	53	75 2,3 B	67 4-7 A
59	52	53	75 4,5 B	67 8-11 A
60	52	53	75 6,7 B	67 12-15 A
61	52	53	75 8,9 B	67 0-3 B

Table I (Concluded)

Device Code Assignments

Connector	ALU/SLU RCV	ALU/SLU XMT	Digital* Input		Digital* Output	
62	52	53	75	10,11 B	67	4-7 B
63	52	53	75	12,13 B	67	8-11 B
64	52	53	75	14,15 B	67	12-15 B
65	54	55	76	0,1 A	70	0-3 A
66	54	55	76	2,3 A	70	4-7 A
67	54	55	76	4,5 A	70	8-11 A
68	54	55	76	6,7 A	70	12-15 A
69	54	55	76	8,9 A	70	0-3 B
70	54	55	76	10,11 A	70	4-7 B
71	54	55	76	12,13 A	70	8-11 B
72	54	55	76	14,15 A	70	12-15 B
73	56	57	76	0,1 B	71	0-3 A
74	56	57	76	2,3 B	71	4-7 A
75	56	57	76	4,5 B	71	8-11 A
76	56	57	76	6,7 B	71	12-15 A
77	56	57	76	8,9 B	71	0-3 B
78	56	57	76	10,11 B	71	4-7 B
79	56	57	76	12,13 B	71	8-11 B
80	56	57	76	14,15 B	71	12-15 B

* The "A" or "B" appended to the bit numbers denotes whether the line is controlled by a DIA (DOA) or DIB (DOB) instruction.

WIRING LIST

Sheet 1

TITLE: Typical Interface Panel Jumper Connections

SYSTEM: On-Site NOVA

NOTES: This jumper arrangement will provide all the necessary EIA RS232C signals for most low and high speed modems. Wiring is identical for all 16 B.S.

FROM Barrier Strip A **TO** Barrier Strips B and Clock

FROM	TO	SIGNAL NAME	FROM	TO	SIGNAL NAME
Terminal	Terminal				
1	2	Transmit Data			
2	3	Receive Data			
3	6	Data Set Ready			
4	8	Received Line Signal Detector			
5	22	Ring Indicator			
6	5	Clear to send			
9	15 & BSC 1-8	Transmission Signal Element Timing (DCE Source)			
10	17 & BSC 1-8	Receiver Signal Element Timing (DCE Source)			
7	4	Request to Send			
8	20	Data Terminal Ready			

WIRING LIST

Sheet 2

TITLE: Modem Clock Cable

SYSTEM: On-Site Nova

NOTES: Connectors are Cinch DD-155. Cable is shielded. Shield is connected to pins 14 and 15 at both ends.

FROM Connector **TO** Connector

FROM Pin	TO Pin	SIGNAL NAME		FROM	TO	SIGNAL NAME
1	1	9600				
2	2	4800				
3	3	2400				
4	4	1800				
5	5	1200				
6	6	600				
7	7	300				
8	8	150				
9	9					
10	10	Positive, EIA Power				
11	11	Negative, EIA Power				
12	12	LED Power				
13	13	LED Ground				
14	14	Signal Ground				
15	15	Signal Ground				

WIRING LIST

Sheet 3

TITLE: Interface Panel Back Connector S4

SYSTEM: On-Site Emulator

NOTES: S4 contains the timing signals that are needed by the NOVA synchronous line adapters.

FROM Socket S4 **TO** Barrier Strips A

FROM	TO	SIGNAL NAME		FROM	TO	SIGNAL NAME
Pin	Terminal	Clock Signals		27	BSA14, 9	
1	BSA1, 9	Transmit		28	BSA14,10	
2	BSA1, 10	Receive		29	BSA15, 9	
3	BSA2, 9			30	BSA15,10	
4	BSA2, 10			31	BSA16, 9	
5	BSA3, 9			32	BSA16,10	
6	BSA3, 10					
7	BSA4, 9					
8	BSA4, 10					
9	BSA5, 9					
10	BSA5, 10					
11	BSA6, 9					
12	BSA6, 10					
13	BSA7, 9					
14	BSA7, 10					
15	BSA8, 9					
16	BSA8, 10					
17	BSA9, 9					
18	BSA9, 10					
19	BSA10, 9					
20	BSA10,10					
21	BSA11, 9					
22	BSA11,10					
23	BSA12, 9					
24	BSA12,10					
25	BSA13, 9					
26	BSA13,10					

WIRING LIST

Sheet 4

TITLE: Interface Panel Back Connector S5

SYSTEM: On-Site Emulator

NOTES: S5 contains the data signals

FROM Socket S5 TO Barrier Strips A

FROM	TO	SIGNAL NAME		FROM	TO	SIGNAL NAME
Pin	Terminal			27	BSA14, 1	
1	BSA1, 1	Transmit Data		28	BSA14, 2	
2	BSA1, 2	Receive Data		29	BSA15, 1	
3	BSA2, 1			30	BSA15, 2	
4	BSA2, 2			31	BSA16, 1	
5	BSA3, 1			32	BSA16, 2	
6	BSA3, 2					
7	BSA4, 1					
8	BSA4, 2					
9	BSA5, 1					
10	BSA5, 2					
11	BSA6, 1					
12	BSA6, 2					
13	BSA7, 1					
14	BSA7, 2					
15	BSA8, 1					
16	BSA8, 2					
17	BSA9, 1					
18	BSA9, 2					
19	BSA10, 1					
20	BSA10, 2					
21	BSA11, 1					
22	BSA11, 2					
23	BSA12, 1					
24	BSA12, 2					
25	BSA13, 1					
26	BSA13, 2					

WIRING LIST

Sheet 5

TITLE: Interface Panel Back Connector S6

SYSTEM: On-Site Emulator

NOTES: S6 contains clock and power signals

FROM Socket S6 TO Barrier Strips C1, C2

FROM	TO	SIGNAL NAME		FROM	TO	SIGNAL NAME
Pin	Terminals					
1	BSC1, 1	9600				
2	BSC1, 2	4800				
3	BSC1, 3	2400				
4	BSC1, 4	1800				
5	BSC1, 5	1200				
6	BSC1, 6	600				
7	BSC1, 7	300				
8	BSC1, 8	150				
9						
10	BSC2, 6	Positive EIA Power				
11	BSC2, 7	Negative EIA Power				
12	BSC2, 8	LED Power				
13	BSC2, 9	LED Ground				
14	BSC1, 10	Signal Ground				
15	BSC2, 10	Signal Ground				

WIRING LIST

Sheet 6

TITLE: Interface Panel Front Connectors

SYSTEM: On-Site Emulator

NOTES: Signal Names are given as the EIA RS232 standard specifies, since most interfaces will conform to this standard. All 16 connectors are wired identically.

FROM 25 Pin Connector **TO** Barrier Strip B

FROM	TO	SIGNAL NAME		FROM	TO	SIGNAL NAME
Pin	Terminal	(EIA RS232)				
1		Protective Ground				
2	2	Transmitted Data				
3	3	Received Data				
4	4	Request to Send				
5	5	Clear to Send				
6	6	Data Set Ready				
7	7	Signal Ground (Common Return)				
8	8	Received Line Signal Detector				
9	9					
10	10					
11	11					
12	12	Secondary Received Line Signal Detector				
13	13	Secondary Clear to Send				
14	14	Secondary Transmitted Data				
15	15	Transmission Signal Element Timing (DCE Source)				
16	16	Secondary Received Data				
17	17	Receiver Signal Element Timing (DCE Source)				
18	18					
19	19	Secondary Request to Send				
20	20	Data Terminal Ready				
21	21	Signal Quality Detector				
22	22	Ring Indicator				
23	23	Data Signal Rate Selector (DTE/DCE Source)				
24	24	Transmit Signal Element Timing (DTE Source)				
25	25					

WIRING LIST

Sheet 7

TITLE: Interface Panel Back Connector S3

SYSTEM: On-Site Emulator

NOTES: S3 contains the digital input signals for the front panel connectors.

FROM Socket S3 TO Barrier Strips A

FROM	TO	SIGNAL NAME		FROM	TO	SIGNAL NAME
Pin	Terminal	Digital Inputs		27	BSA14, 7	
1	BSA1, 7			28	BSA14, 8	
2	BSA1, 8			29	BSA15, 7	
3	BSA2, 7			30	BSA15, 8	
4	BSA2, 8			31	BSA16, 7	
5	BSA3, 7			32	BSA16, 8	
6	BSA3, 8					
7	BSA4, 7					
8	BSA4, 8					
9	BSA5, 7					
10	BSA5, 8					
11	BSA6, 7					
12	BSA6, 8					
13	BSA7, 7					
14	BSA7, 8					
15	BSA8, 7					
16	BSA8, 8					
17	BSA9, 7					
18	BSA9, 8					
19	BSA10, 7					
20	BSA10, 8					
21	BSA11, 7					
22	BSA11, 8					
23	BSA12, 7					
24	BSA12, 8					
25	BSA13, 7					
26	BSA13, 8					

WIRING LIST

Sheet 8

TITLE: Interface Panel Back Connectors S2

SYSTEM: On-Site Emulator

NOTES: S2 contains the digital output signals for the last eight front panel connectors.

FROM Socket S2 **TO** Barrier Strips A

FROM	TO	SIGNAL NAME		FROM	TO	SIGNAL NAME
Pin	Terminal	Digital Outputs		27	BSA7, 5	
1	BSA1, 3			28	BSA7, 6	
2	BSA1, 4			29	BSA8, 3	
3	BSA1, 5			30	BSA8, 4	
4	BSA1, 6			31	BSA8, 5	
5	BSA2, 3			32	BSA8, 6	
6	BSA2, 4					
7	BSA2, 5					
8	BSA2, 6					
9	BSA3, 3					
10	BSA3, 4					
11	BSA3, 5					
12	BSA3, 6					
13	BSA4, 3					
14	BSA4, 4					
15	BSA4, 5					
16	BSA4, 6					
17	BSA5, 3					
18	BSA5, 4					
19	BSA5, 5					
20	BSA5, 6					
21	BSA6, 3					
22	BSA6, 4					
23	BSA6, 5					
24	BSA6, 6					
25	BSA7, 3					
26	BSA7, 4					

WIRING LIST

Sheet 9

TITLE: Interface Panel Back Connector S1

SYSTEM: On-Site Emulator

NOTES: S1 contains the digital output signals for the first eight front panel connectors.

FROM Socket S1 **TO** Barrier Strips A

FROM	TO	SIGNAL NAME		FROM	TO	SIGNAL NAME
Pin	Terminal	Digital Outputs		27	BSA15, 5	
1	BSA9, 3			28	BSA15, 6	
2	BSA9, 4			29	BSA16, 3	
3	BSA9, 5			30	BSA16, 4	
4	BSA9, 6			31	BSA16, 5	
5	BSA10,3			32	BSA16, 6	
6	BSA10,4					
7	BSA10,5					
8	BSA10,6					
9	BSA11,3					
10	BSA11,4					
11	BSA11,5					
12	BSA11,6					
13	BSA12,3					
14	BSA12,4					
15	BSA12,5					
16	BSA12,6					
17	BSA13,3					
18	BSA13,4					
19	BSA13,5					
20	BSA13,6					
21	BSA14,3					
22	BSA14,4					
23	BSA14,5					
24	BSA14,6					
25	BSA15,3					
26	BSA15,4					

WIRING LIST

Sheet 10

TITLE: Digital Output Boards Back Panel Wiring

SYSTEM: On-Site NOVA

NOTES: These connections are between each digital output board and the connector for the cable to the interface adapter rack.

FROM Digital Output Boards Back Panel **TO** Digital Output Cable Connectors

FROM	TO	SIGNAL NAME	FROM	TO	SIGNAL NAME
1	1	Digital Output Ø	28	28	
2	2	Digital Output 1	29	29	Digital Output Ø
3	3	Digital Output 2	30	30	Digital Output 1
4	4	Digital Output 3	31	31	Digital Output 2
5	5		32	32	Digital Output 3
6	6		50	50	Signal ground
7	7				
8	8				
9	9				
10	10				
11	11				
12	12				
13	13				
14	14				
15	15				
16	16				
17	17				
18	18				
19	19				
20	20				
21	21				
22	22				
23	23				
24	24				
25	25				
26	26				
27	27				

WIRING LIST

Sheet 11

TITLE: Digital Input Board Back Panel Wiring

SYSTEM: On-Site NOVA

NOTES: These connections are between each digital input board and the connector for the cable to the interface adapter rack.

FROM Digital Input Boards Back Panel **TO** Digital Input Cable Connectors

FROM	TO	SIGNAL NAME	FROM	TO	SIGNAL NAME
1	1	Digital Input 0	28	28	
2	2	Digital Input 1	29	29	
3	3		30	30	
4	4		31	31	Digital Input 0
5	5		32	32	Digital Input 1
6	6		50	50	Signal Ground
7	7				
8	8				
9	9				
10	10				
11	11				
12	12				
13	13				
14	14				
15	15				
16	16				
17	17				
18	18				
19	19				
20	20				
21	21				
22	22				
23	23				
24	24				
25	25				
26	26				
27	27				

WIRING LIST

Sheet 12

TITLE: Synchronous Data Line Back Panel Connectors

SYSTEM: On-Site NOVA

NOTES: These connections are between each SLU and the connector for the cable to the interface adapter rack. Two SLU boards share one connector.

FROM SLU data cable **TO** NOVA Back Panel of SLU

FROM	TO	SIGNAL NAME		FROM	TO	SIGNAL NAME
1	15-B91	XMT 0				
2	15-B40	RCV 0				
3	15-B9	XMT 1				
4	15-B15	RCV 1				
5	15-A65	XMT 2				
6	15-A63	RCV 2				
7	15-A71	XMT 3				
8	15-A84	RCV 3				
9	17-B91	XMT 0				
10	17-B40	RCV 0				
11	17-B9	XMT 1				
12	17-B15	RCV 1				
13	17-B65	XMT 2				
14	17-B63	RCV 2				
15	17-A71	XMT 3				
16	17-A84	RCV 3				
47	A1	GND				
48	A1	GND				
49	A100	GND				
50	A100	GND				

WIRING LIST

Sheet 13

TITLE: Synchronous Clocking Signals; Back Panel Connectors

SYSTEM: On-Site NOVA

NOTES: These connections are between each SLU and the connector for the cable to the interface adapter rack. Two SLU boards share one connector.

FROM SLU Timing Cahle **TO** NOVA Back Panel of SLU's

FROM	TO	SIGNAL NAME		FROM	TO	SIGNAL NAME
1	15-B53	XMT CLK Ø				
2	15-B49	RCV CLK Ø				
3	15-B54	1				
4	15-B52	1				
5	15-A59	2				
6	15-A69	2				
7	15-A85	3				
8	15-A83	3				
9	17-B53	0				
10	17-B49	0				
11	17-B54	1				
12	17-B52	1				
13	17-A59	2				
14	17-A69	2				
15	17-A85	XMT CLK 3				
16	17-A83	RCV CLK 3				
47		GND				
48		GND				
49		GND				
50		GND				

WIRING LIST

Sheet 14

TITLE. 32 Line Cable

SYSTEM: On-Site Emulator

NOTES: Connectors are Cinch type DD-50P. Cable is shielded. Shield is connected to shield ground pins at both connectors. These cables provide the connection between the NOVA and the interface adapter rack.

FROM Connector TO Connector

FROM	TO	SIGNAL NAME		FROM	TO	SIGNAL NAME
1	1			28	28	
2	2			29	29	
3	3			30	30	
4	4			31	31	
5	5			32	32	
6	6			33	33	Signal Ground
7	7			34	34	Signal Ground
8	8			35	35	Signal Ground
9	9			36	36	Signal Ground
10	10			37	37	Signal Ground
11	11			38	38	Signal Ground
12	12					
13	13			48	48	Shield Ground
14	14			49	49	Shield Ground
15	15			50	50	Shield Ground
16	16					
17	17					
18	18					
19	19					
20	20					
21	21					
22	22					
23	23					
24	24					
25	25					
26	26					
27	27					

WIRING LIST

Sheet 15

TITLE: Asynchronous Line Unit Back Panel Wiring

SYSTEM: On-Site NOVA

NOTES: These connections are between each ALU and the connector for the cable to the interface adapter rack. Note that one 50 pin connector is fed from two ALU boards.

FROM NOVA Back Panel ofALU's **TO** ALU Data Cable

FROM	TO	SIGNAL NAME	FROM	TO	SIGNAL NAME
XA 47	1	XMT	YB 25	24	RCV
XA 49	2	RCV	YB 31	27	XMT
XA 59	6	XMT	YB 49	28	RCV
XA 63	5	RCV	YB 51	31	XMT
XA 67	9	XMT	YB 67	32	RCV
XA 69	10	RCV	XA1	47	GND
XA 73	13	XMT	YA1	48	GND
XA 75	14	RCV	XA 100	49	GND
XB 13	3	XMT	YA 100	50	GND
XB 15	4	RCV			
XB 19	7	XMT			
XB 25	8	RCV			
XB 31	11	XMT			
XB 49	12	RCV			
XB 51	15	XMT			
XB 67	16	RCV			
YA 47	17	XMT			
YA 49	18	RCV			
YA 59	22	XMT			
YA 63	21	RCV			
YA 67	25	XMT			
YA 69	26	RCV			
YA 73	29	XMT			
YA 75	30	RCV			
YB 13	19	XMT			
YB 15	20	RCV			
YB 19	23	XMT			

APPENDIX B

MODEM CLOCKS

The modem clocks produce signals at eight frequencies for use as clocking pulses for synchronous communication. The eight frequencies are shown in Table II.

Table II

Modem Clock Frequencies (Hz)

9600
4800
2400
1800
1200
600
300
150

The signals are all available simultaneously and their frequencies are crystal controlled for a high degree of accuracy and stability. The output signals from the clock conform to EIA standard RS232C, delivering over 20 volt peak-to-peak signals with no load and approximately 5 volts into a 10 ohm load. The outputs may be grounded or shorted to each other without damage. The frequencies may be adjusted by approximately $\pm$.002% by an internal adjustment.

The clock consists of three basic sections: a crystal oscillator, a frequency divider, and output buffer amplifiers. To synthesize the eight frequencies, a crystal oscillator produces a 460.8 kHz signal. Dividing by 16 produces 28.8 kHz. Further dividing produces the output frequencies. The division of the 460.8 kHz oscillator frequency required to produce the output frequency is shown in Table III.

Table III

Frequency Synthesis

Synthesized Frequency (Hz)	460.8 kHz Division Factor
9600	48
4800	96
2400	192
1800	256
1200	384
600	768
300	1536
150	3072

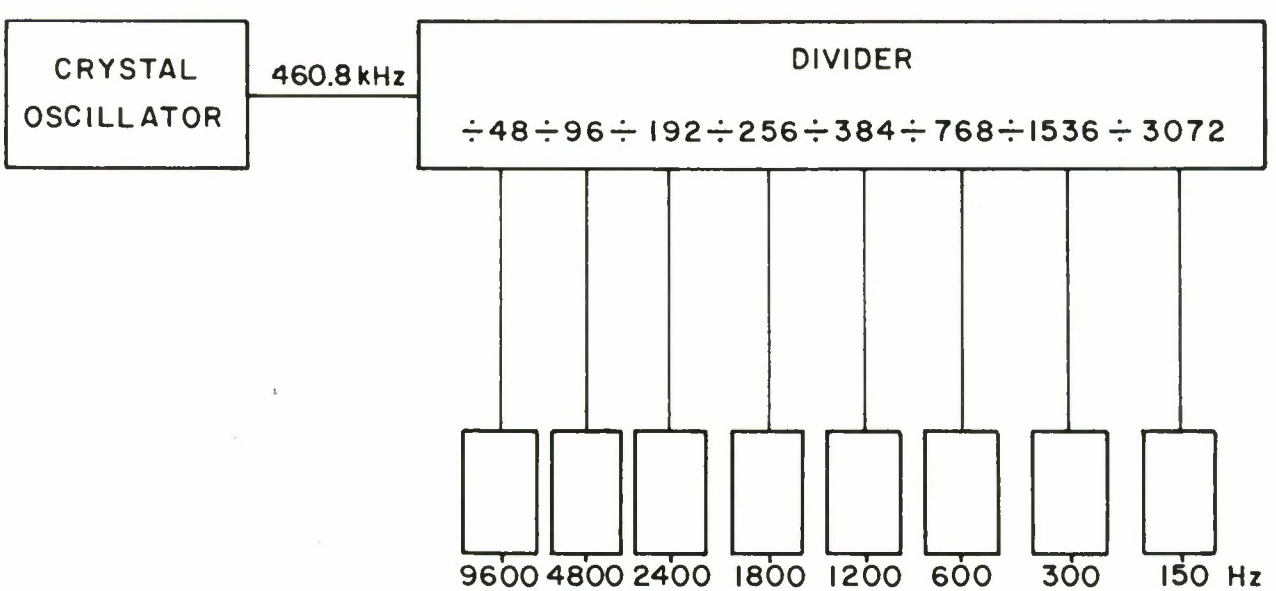


Figure 12. Simplified Diagram of the Modem Clocks

The output frequencies are then amplified by buffer amplifiers that can supply the desired output power. Figure 12 shows a block diagram of the modem clock.

Circuit Description

Figure 13 is a schematic diagram of the modem clock circuit. The NE510A Dual Operational Amplifier provides two stages of gain for the oscillator. The 460.8 kHz crystal tunes the positive-feedback path, which insures stable operation. The transistor amplifier voltage divider and the inverter couple the clock signal into the frequency divider network. The first divider I.C. (a 7493) lowers the frequency to 28.8 kHz.

The path then splits with the 28.8 kHz going to another 7493 for division by 16 to 1800 Hz, and to a 7492 for division by 3 to provide a 9600 Hz signal. This is then further divided by 2, producing the 4800 Hz and 2400 Hz signals. The 2400 Hz is also used as an input to the final 7493, where four successive divisions by two yield 1200 Hz, 600 Hz, 300 Hz, and 150 Hz.

These eight frequencies from 9600 Hz to 150 Hz are now TTL logic levels (0, +5 volts) and must be converted to EIA signals for use by modems. The 2N3906 and 2N3904 amplify the voltage. This large voltage is further amplified by the MJE1101 and MJE1091 Darlington power transistors, connected as emitter-follower amplifiers. The 10 ohm output resistor provides current-limiting protection for both power supplies.

Construction Parts

All parts are mounted on a wire wrap board except the following:

Y1	Crystal
C1	Variable Capacitor
C3	15 microfarads

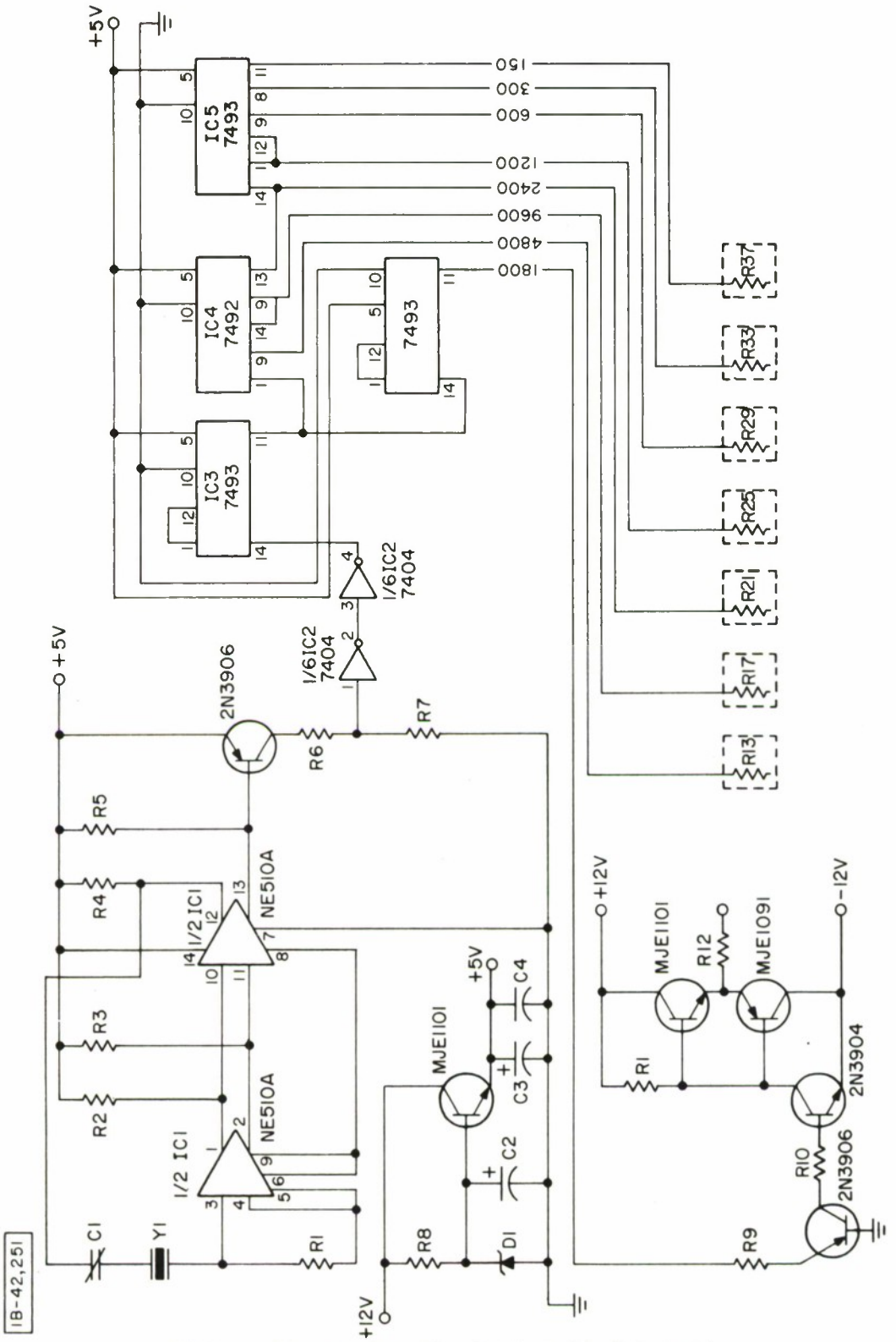


Figure 13. Modem Clock Circuit Schematic

C4 1100 microfarads

All MJE1101 Transistors

All MJE1091 Transistors

All 10 25-watt resistors

IC's are plugged directly into the board. The discrete components are mounted on 14 pin headers, and these are also plugged into the board. +12 and -12 volts are supplied by an Acopian TD12-100 dual 12-volt power supply for which an on/off switch is provided on the front panel. The output transistors and ten current-limiting resistors are mounted on an aluminum heat sink. Some wiring between components is done underneath the aluminum, and connections to the Augat board and output connections are made on the top side. A solder lug bolted to the side of the power supply serves as the system ground. This ground is connected to the power supply line cord.

APPENDIX C

READABLE REAL-TIME CLOCK AND INTERVAL TIMER DOCUMENTATION

This appendix describes the design and implementation of the Readable Real-Time Clock (RRTC) and Interval Timer (IT). These were developed for use with the fixed-site and on-site RTE's in order to increase the precision of event timing and to decrease the overhead on the real-time executive. They were designed by project personnel and implemented on a Data General general-purpose Interface Board (4040).

The design specifications for these two units are given in Table IV.

GENERAL DESCRIPTION

The Readable Real-Time Clock (RRTC) is a 32-bit binary clock; each clock count represents ten microseconds. The clock can be reset to zero, a clock reading can be stored in the RRTC output buffers, and the present clock reading or the stored reading can be loaded into any of the computer's accumulators under program control.

The basic operation of the RRTC is shown by the block diagram in Figure 14. The clock signal is a square wave generated by a crystal oscillator. On the clock signal's negative-transition, the output buffers are strobed (via the oneshot) to receive the new clock count. Thus, the counter is allowed five microseconds to settle before its output is placed into the output buffers.

THEORY OF OPERATION OF THE RRTC AND IT

The execution of a Data In A or a Data In B instruction by the computer generates pulses on the $\overline{\text{DATA IN A}}$ or $\overline{\text{DATA IN B}}$ lines (where the overlines indicate negative true levels). These pulses gate the

Table IV

Specifications for the RRTC and IT

GENERAL	
Physical:	Both the RRTC and the IT are constructed on the same Data General 4040 General Purpose Interface Board equipped with option 4044. The board occupies one sub-assembly slot.
Hardware:	The 4040 Interface Board is wired to respond to Device Code 33, to respond to an Interrupt Acknowledge Instruction with Device Code 33, and to recognize bit 7 during a Mask Out instruction to disable its interrupt request flip flop.
Software:	The crystal oscillator has been adjusted to 100,000.1 Hz at 110°F. Temperature tests showed that the oscillator's frequency remained at this value from 80°F to 115°F. The average frequency drift from 55°F was measured at .04 Hz/F°.
RRTC SPECIFICATIONS	
Maximum Count:	37777777777_8; 42949.67295 seconds; approximately 11.930 hours.
Each Count:	10 microseconds.
Software Control:	The counter can be set to zero by executing a Data Out C instruction. The contents of the accumulator specified by this instruction are unaffected and not used.

Table IV (Continued)

Specifications for the RRTC and IT

	The 16 least significant bits (as held in output buffer A) can be transferred to any accumulator by executing a Data In A instruction. The 16 most significant bits (as held in output buffer B) can be transferred to any accumulator by executing a Data In B instruction. These instructions also freeze the data in both output buffers. Issuance of an I/O pulse will allow the buffers to continue being updated with each count. The I/O pulse can be issued with the Data In A or Data In B instruction or at a later time. Issuance of an I/O pulse insures that the output buffers will be updated within 6 microseconds following the pulse. The S and C functions are illegal for the RRTC since they affect the operation of the Interval Timer.
IT SPECIFICATIONS	
Maximum Count:	177777_8; 65.535 seconds.
Each Count:	1.0 millisecond.
Software Control:	A Data OUT A instruction loads the Interval Timer with the contents of the specified accumulator.

Table IV (Concluded)

Specifications for the RRTC and IT

	The Data In C instruction reads the output buffer into the specified accumulator. The P function is illegal for the IT since it affects the operation of the RRTC. The S and C functions have the standard effect upon Busy and Done flip flops. The C function also clears the Interval Timer. Loading zero into the IT sets Busy (if Busy is not already set) and will cause Done to be set within 10 microseconds.

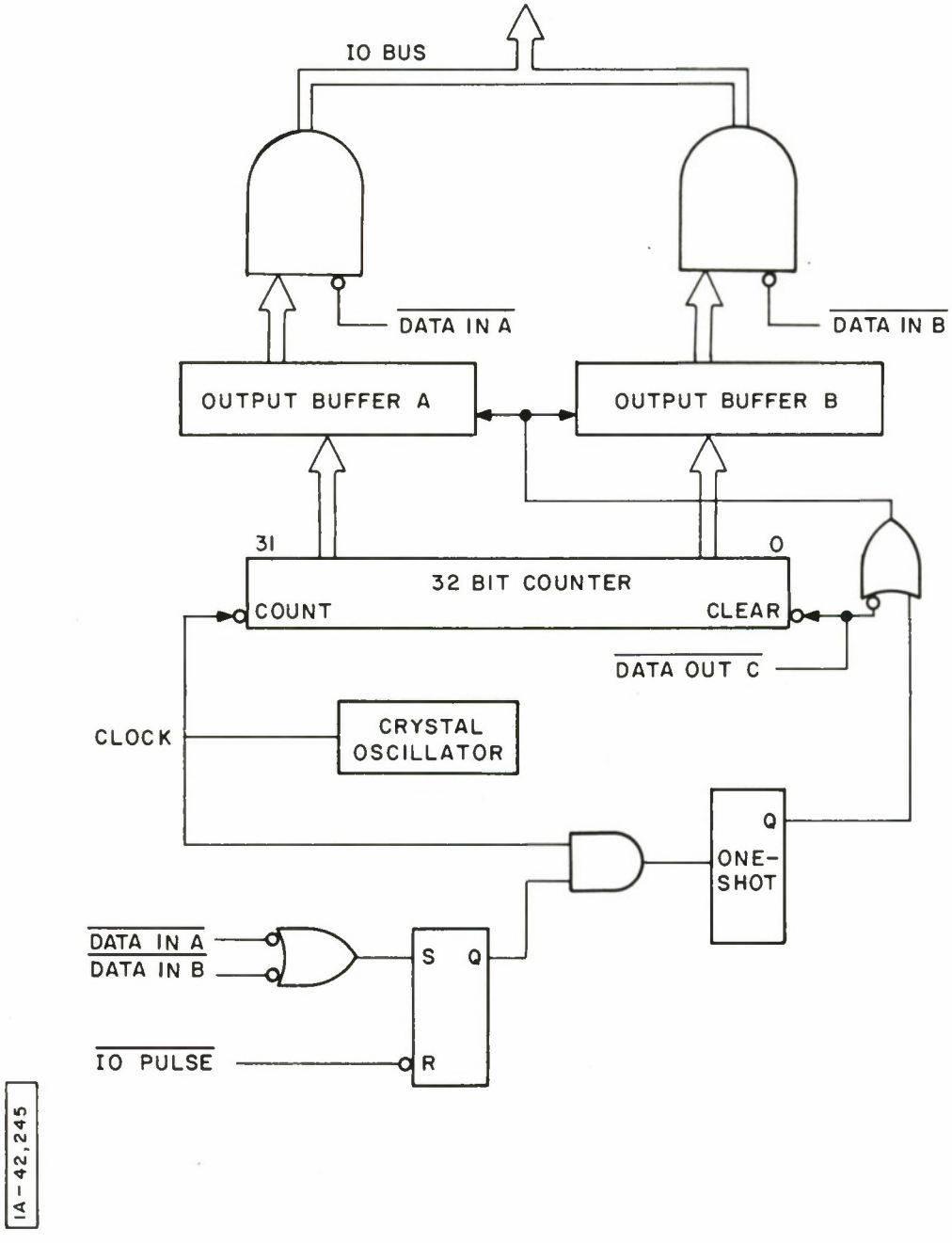


Figure 14. Readable Real-Time Clock Block Diagram

data in the output buffers onto the I/O bus. In addition, they set the RS flip flop. This flip flop prevents the output buffers from being updated while they are being gated onto the I/O bus. The RS flip flop can only be reset by an I/O pulse ($\overline{\text{I/O PULSE}}$). Thus, the output buffers can be used to retain timing data for any desired period. If an I/O pulse is generated by each Data In instruction (allowing only half the clock to be read), then the RS flip flop would reset at the end of the instruction cycle, thus ensuring that the current count is always available in the output buffers.

The 32-bit counter will continue to count with no loss in accuracy during all of the above actions. In fact, the only way to alter the 32-bit counter is to execute a Data Out C instruction. This instruction clears the counter and the output buffers.

The Interval Timer (IT) is a 16-bit binary clock with each clock count representing one millisecond. The IT can be activated for the duration of an interval set by the program; at the end of the interval, the IT will interrupt the computer. The IT can also be read and cleared under program control. In operation, the IT counts down to zero from an initial value set by the program and then halts. The IT will generate an interrupt when it halts if the Busy flip flop has been set and the Interrupt Disable flip flop is clear.

The basic operation of the IT is shown in Figure 15. This block diagram shows that a Data Out A instruction loads the contents of the I/O bus into the down counter and the output buffer. The down counter decrements on each positive going edge of the clock signal's square wave. The positive going edge also fires the "ripple" oneshot. This oneshot produces a pulse of sufficient duration that the counter's output has settled before the trailing edge of the pulse fires the "strobe" oneshot. The output buffer loads in the new count when the "strobe" oneshot fires. The output buffer is read by a Data In C

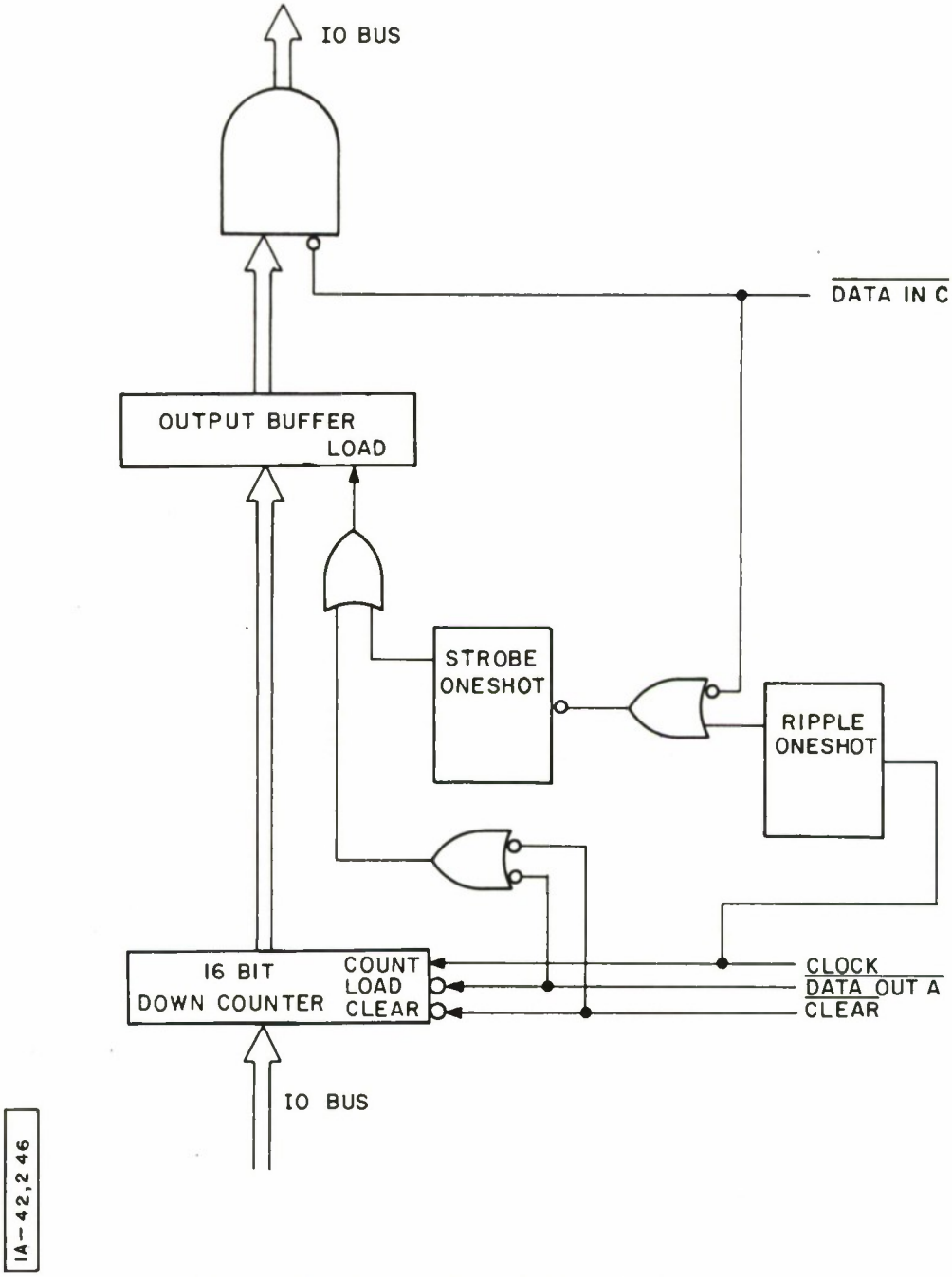


Figure 15. Interval Timer Block Diagram

instruction. This instruction produces the $\overline{\text{DATA IN C}}$ pulse that gates the contents of the output buffer onto the I/O bus and simultaneously disables the "strobe" oneshot so that the output buffer cannot change while it is being read. The down counter and the output buffer can be cleared by issuing a clear pulse ($\overline{\text{CLEAR}}$) to the device.

CIRCUIT DESCRIPTION

The following circuit description references the RRTC and IT schematic diagram, shown in Figure 16, and Data General 4040 General-Purpose Interface (GPI) schematics as shown in "How to Use the NOVA Computers" (see Bibliography). All of the signals shown entering or leaving the RRTC and IT schematic originate or terminate on the 4040 schematic and conform to the Data General nomenclature.

- Oscillator: The crystal oscillator consisting of Y1, IC31, and related components outputs a 100,000 Hz square wave from IC25, pin 6. This self-starting oscillator drives both the RRTC and IT. Note that the IT has two divide-by-ten circuits (IC26, IC54) that output a 1000 Hz square wave to the down counter (IC27-30).

- Multiplexor: NAND gates IC7-IC18 and NOR gates IC1-IC6 form a three-word multiplexor, 16 bits per word. This multiplexor selects which output buffer is gated onto the I/O bus. For example, whenever a Data In A instruction is executed, the resulting $\overline{\text{DATA IN A}}$ signal gates the A buffer into the NOR gates IC-IC6. The outputs of these NOR gates are connected to NAND buffers (on the 4040 GPI board) which drive the I/O bus data lines.

- 32-Bit Binary Counter: The four-bit binary counters IC46-IC53 form a 32-bit binary counter. IC46, pin 14 is connected to the RRTC CLOCK signal and counts on the negative going edge of

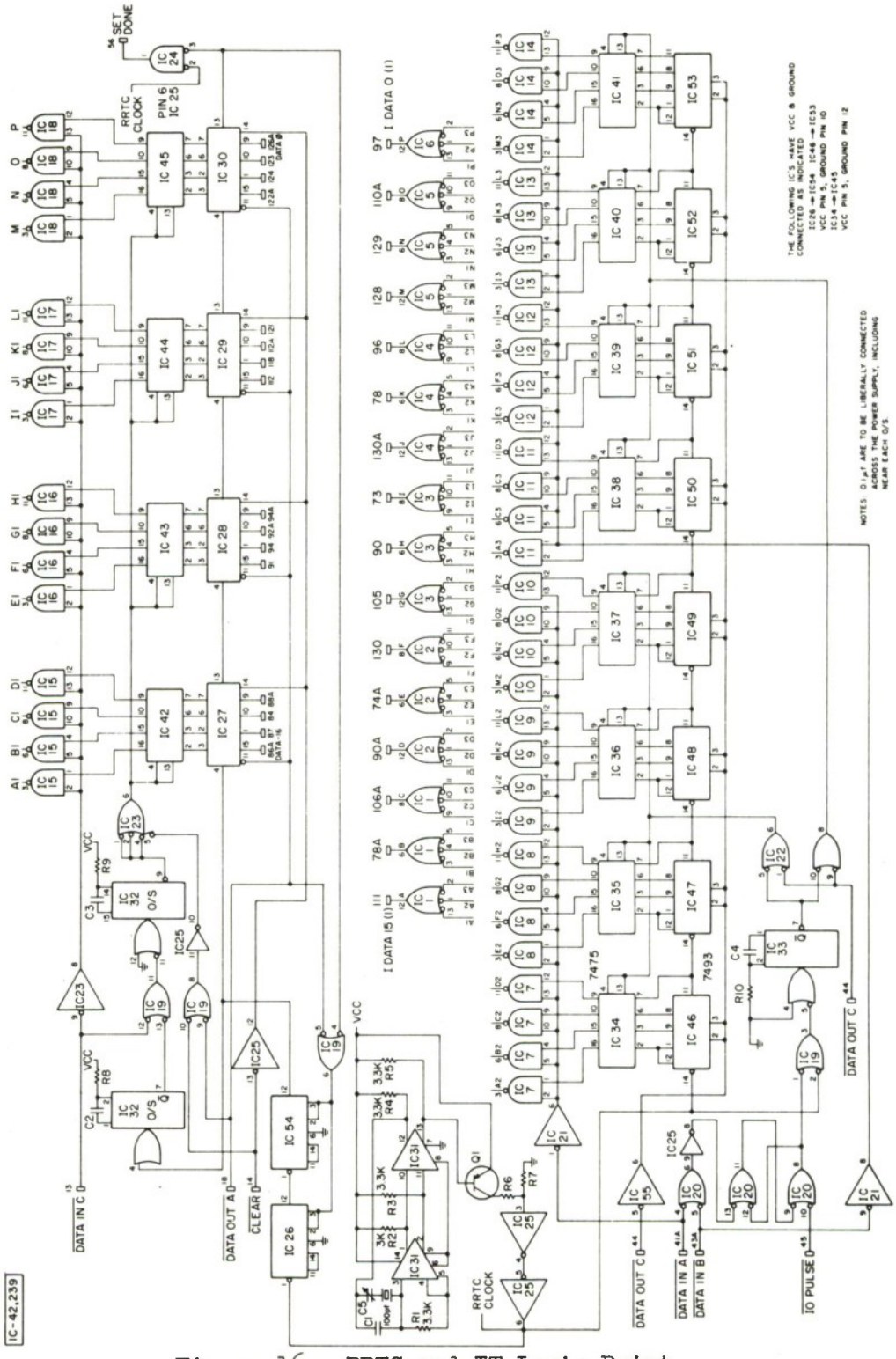


Figure 16. RRTC and IT Logic Print

this signal. Pin 11 of this IC is its most significant bit and is connected to the input of the next four-bit counter. Thus, whenever IC46 counts from 1111 to 0000, then IC47, pin 14 sees a negative going edge and counts one count. The other four-bit counters are similarly connected. When the counter overflows, the count sequence simply starts over. The counter is reset to zero if a Data Out C instruction occurs. This instruction generates the $\overline{\text{DATA OUT C}}$ pulse which clears IC46-IC53 via pins 2 and 3 and loads all zeros into IC34-IC41.

- RRTC Output Buffers: The quad latches IC34-IC41 form two output buffers. These buffers serve a dual function as both holding registers and guaranteed stable output registers. When the RRTC CLOCK signal goes positive, IC19, pin 3 goes negative, triggering the oneshot IC33. IC33's output is buffered and then used to gate the inputs to the quad latches (pins 2, 3, 6, 7) onto the outputs (pins 16, 15, 10, 9). Since the 32-bit counter increments when RRTC CLOCK goes negative, the counter ripple has ample time to propagate and settle before the new count is gated into the quad latches.

- RS Flip Flop: One half of IC20 is connected as an RS flip flop. If pin 11 of IC20 is considered as the Q output, then $\overline{\text{DATA IN A}}$ or $\overline{\text{DATA IN B}}$ sets the flip flop and $\overline{\text{I/O PULSE}}$ clears it. When set, IC20, pin 8 will be low, forcing IC19, pin 3 high independently of the input of IC19, pin 2. Thus, IC33 can not be triggered when the RS flip flop is set. As a result, the output buffers will hold the count that was last gated to them. This guarantees that stable data is presented to the I/O bus and additionally, that both output buffers can be read without the possibility that the buffers could be updated sometime between the execution of the two necessary Data In instructions. However, the output buffers can be cleared with the RS flip flop set.

- IT Down Counter: The four down counters, IC27-IC30, form a 16-bit down counter. These IC's can be set to the levels on input pins 15, 1, 10, 9 by the $\overline{\text{DATA OUT A}}$ signal. The input pins connect to the I/O bus via the 4040 board, thus allowing a Data Out A instruction to load an interval into the counter. The $\overline{\text{DATA OUT A}}$ signal also clears the divide by 100 circuits (IC26, IC54). This insures that the first count will occur ½ millisecond after loading and that when 000001 is loaded, the interrupt will occur in one millisecond. (It also insures that certain types of scheduling software will statistically have no net loss in accuracy when the IT is read and reset repeatedly.)

Figure 17 and 18 are RRTC and IT timing diagrams. Figure 19 shows the customer section only of the Data General 4040 General-Purpose Board. Pin 1 of all integrated circuits are inserted in the lower right hand receptable of the 16-pin sockets. The socket pins are then labeled according to the integrated circuit placed in each socket. Thus 14-pin IC's force a relabeling of the 16-pin sockets.

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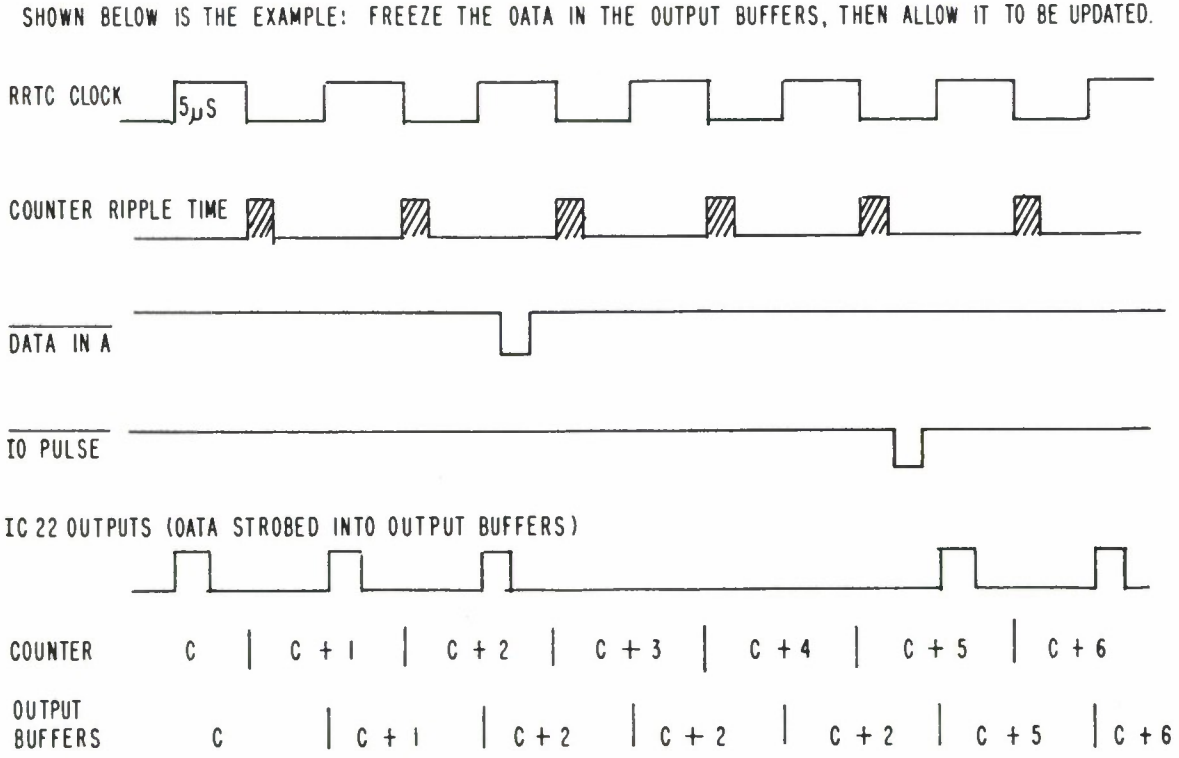

Figure 17. RRTC Timing Diagram

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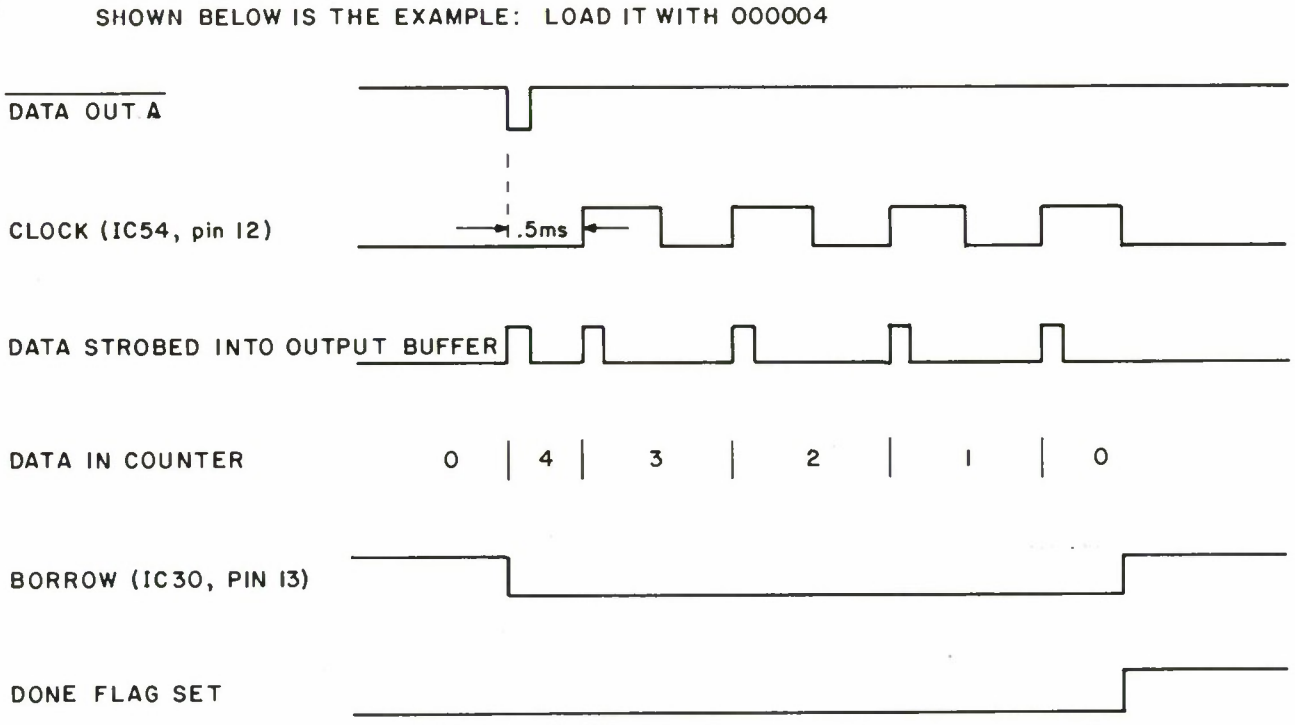

Figure 18. IT Timing Diagram

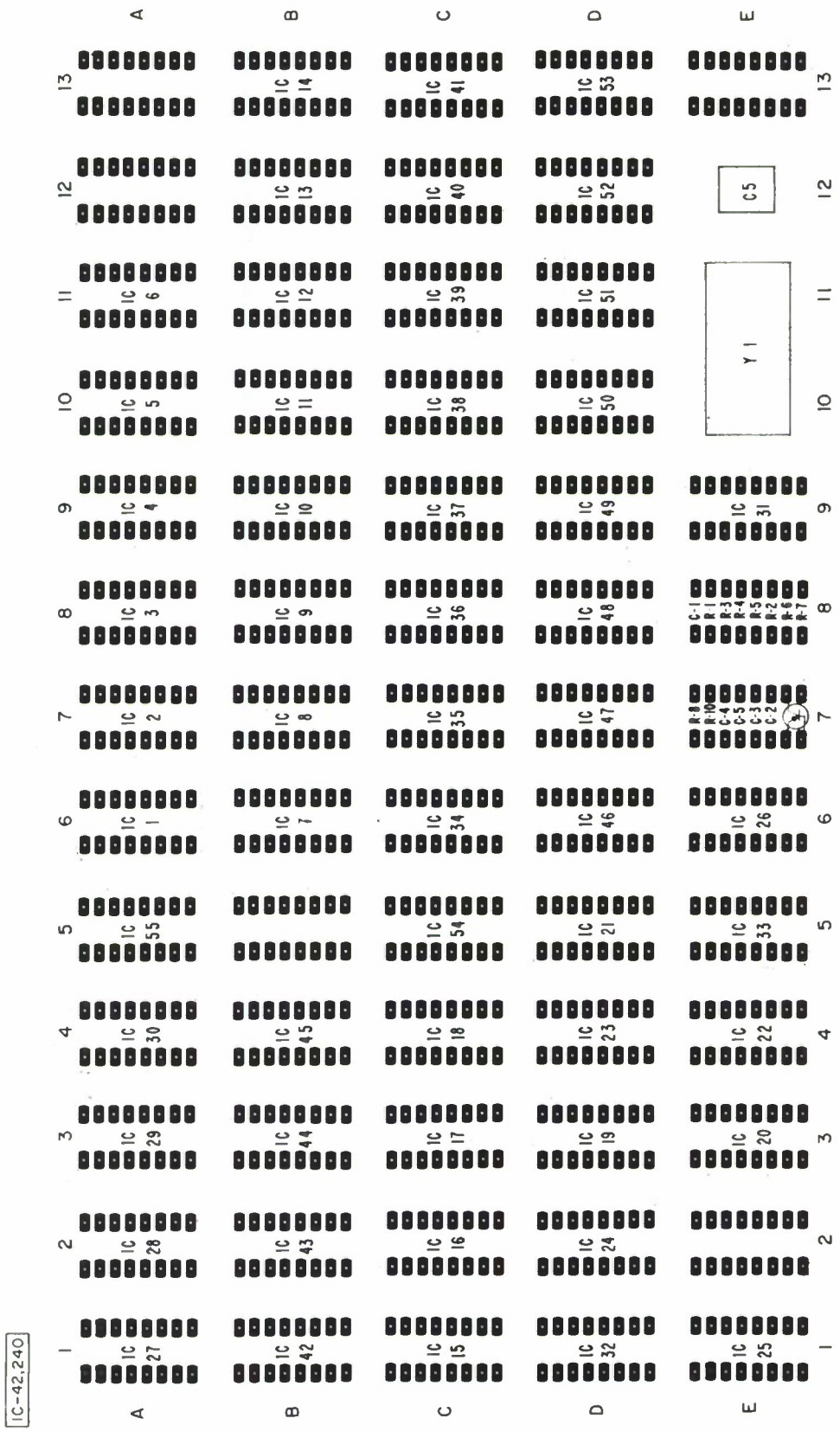

Figure 19. RRTC and IT Assembly Drawing

APPENDIX D

BOARD PLACEMENT AND EQUIPMENT LISTS

BOARD PLACEMENT FOR THE FIXED-SITE SYSTEM

Main Chassis	
17	RRTC and IT
16	4030 Mag Tape Controller
15	4019 Disk Controller
14	4026 16 Line Data Communication Multiplexor
13	4016 Card Reader Controller
12	4034 Line Printer Controller
11	4029 Asynchronous Line Adapter
10	4015 Synchronous Line Adapter
9	4040 General-Purpose Interface Board*
8	
7	8215 8KW Memory
6	8215 8KW Memory
5	8215 8KW Memory
4	8215 8KW Memory
3	4007 HSPTR and Teletype Controller, RTC
2	CPU 2
1	CPU 1

* Used for other applications.

BOARD PLACEMENT FOR ON-SITE SYSTEM

Main Chassis	
17	4 Line Synchronous Line Adapter
16	4034 Line Printer Controller
15	4 Line Synchronous Line Adapter
14	8 Line Asynchronous Line Adapter
13	8 Line Asynchronous Line Adapter
12	RRTC and IT
11	8203 4K Core Memory
10	8203 4K Core Memory
9	8203 4K Core Memory
8	4019 Disk Controller
7	4030 Mag Tape Controller
6	8203 4K Core Memory
5	8203 4K Core Memory
4	8215 8K Core Memory
3	4007 HSPTR and Teletype Controller, RTC
2	CPU 2
1	CPU 1
Expansion Chassis	
7	Spare
6	8 Line Asynchronous Line Adapter
5	8 Line Asynchronous Line Adapter
4	8 Line Asynchronous Line Adapter
3	8 Line Asynchronous Line Adapter
2	8 Line Asynchronous Line Adapter
1	8 Line Asynchronous Line Adapter

Equipment Common to On-Site and Fixed-Site Systems

Equipment	Manufacturer	Model Number	Options	Octal Device Code
NOVA 800 Jumbo CPU	Data General	8239	8208,8222 8224,8159	77
I/O Interface Sub-Assembly	Data General	4007	4008,4010 4011	
Real Time Clock	Data General			14
Magnetic Tape Controller	Data General	4030		
Magnetic Tape Adapter	Data General	4035		
Line Printer Controller	Data General	4034		
Disk Controller	Data General	4019		
Magnetic Tape Transport	Wang Corp.	4030J		22
Line Printer	Data Products	4034A		17
Fixed Head Disk	Data General	6002		20
4KW Core Memory	Data General	8203		
8KW Core Memory	Data General	8215		
Paper Tape Reader	Digitronics	6013		12
Readable Real Time Clock and Interval Timer	MITRE Corp.	-		33
Teletype	Teletype Corp.	ASR-33		10,11

Equipment for Fixed-Site System Only

Equipment	Manufacturer	Model Number	Options
Card Reader Controller	Data General	4036	
Card Reader	Mohawk Data Sciences	4016B	
Digital Comm. MPX	Data General	4026	
High Speed Asynchronous Line Adapter	Data General	4007	4023,4029
Synchronous Line Adapter	Data General	4015	
Modems	Teledynamics	7103F	
Data Access Arrangements	Bell Telephone	1000CDT	

Equipment for On-Site NOVA

Equipment	Manufacturer	Model Number	Options
Interface Rack	MITRE Corp.		
Asynchronous Line Units(8)	Digital Comp. Controls	116474	
Synchronous Line Units (2)	Digital Comp. Controls	116475	
Expansion Chassis	Data General	8024	
Digital Input Lines (160)	Data General	Spec. Prod.	
Digital Output Lines (320)	Data General	Spec. Prod.	

APPENDIX E

POWER AND PHYSICAL REQUIREMENTS FOR NOVA SYSTEMS

CABINET SIZE

Both the on-site and fixed-site systems are contained in standard 19-inch racks. The fixed-site requires two racks (one for the central processor, disk and tape drives, and one for modems and related equipment.) In addition to this, a teletype, card reader, and high speed paper tape reader are mounted in Table top cabinetry. The paper tape reader's cabinet, a "BUD" model, was purchased separately.

The on-site system uses one cabinet for the CPU, digital I/O, and the interface adapter and one cabinet for the tape drive, paper tape reader, and disk. The teletype and line printer are floor consoles.

ENVIRONMENT

Recommended temperature range: from 20°C to 30°C. The relative humidity can reach 90% non-condensing.

POWER REQUIREMENTS

All equipment requires 110-volt (±10%), single-phase power at 47 to 63 Hz.

Equipment	Power Dissipation (Watts)	+ 5 VDC
NOVA 800	350	11 1/4 Amps.
TTY	92	
Line Printer	330	
Card Reader	400	
Tape Drive	475	
Tape Adapter	15	
Disk	200	

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